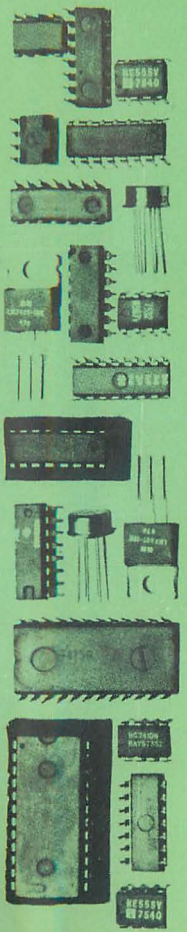
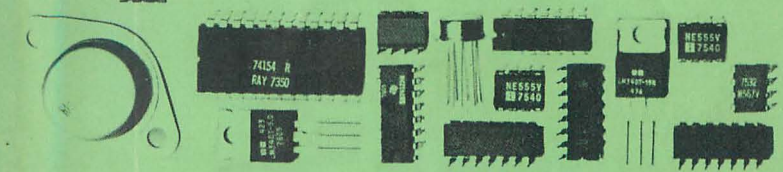
8 1-
SANDY'S
LECTRONICS
$1 98

The Incredible I.C.



The Incredible I.C. line offers the latest in professional quality I.C.'s. This rapidly expanding area of technology offers tremendous opportunities for the hobbyist and experimenter. The Incredible I.C. can be used to create special purpose computers, sophisticated control systems, frequency counters . . . even digital clocks. These semiconductor logic devices function as signal generators; are used as devices for remembering, storing, multiplexing or comparing; and can count, add, subtract, multiply, shift or encode.

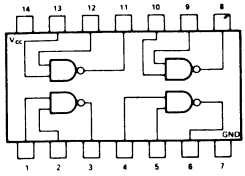
We offer complete lines of the most popular TTL's, linear, CMOS and specialty I.C.'s. All are the top quality available and are offered at prices previously only available to quantity buyers.



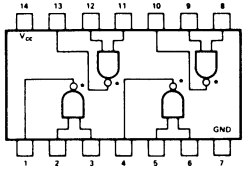
ie, integrated electronics

Integrated Electronics, Inc., P.O. Box 2022, Orange, CA 92669 (714) 997-1673

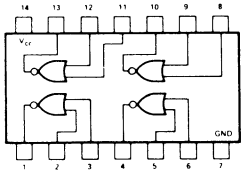
7400 QUADRUPLE 2-INPUT POSITIVE NAND GATE



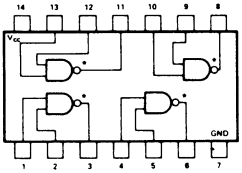
7401 QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT



7402 QUADRUPLE 2-INPUT POSITIVE NOR GATE

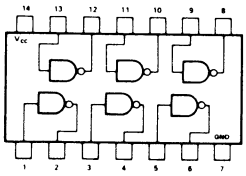


7403 QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

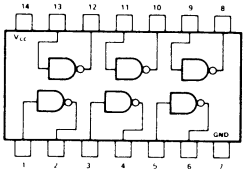


* No pull-up provided

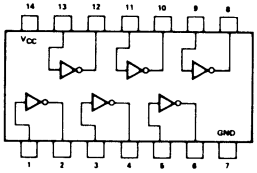
7404 HEX INVERTER



7405 HEX INVERTER WITH OPEN COLLECTOR OUTPUT



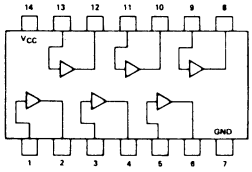
7406 7416 HEX INVERTER BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS



DESCRIPTION

The 54/7406 and 54/7416 Hex Inverter Buffer/Drivers features standard TTL inputs with inverted high voltage, high current, open collector outputs for interface with MOS, lamps or relays. The 54/7406 minimum output breakdown is 30 volts and the 54/7416 minimum output breakdown is 15 volts.

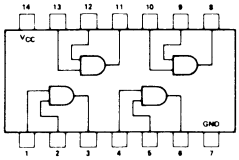
7407 7417 HEX BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS



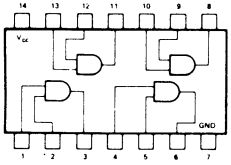
DESCRIPTION

The 54/7407 and 54/7417 Hex Buffer/Driver features standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays. The 54/7407 minimum output is 30 volts and the 54/7417 minimum output is 15 volts.

7408 QUADRUPLE 2-INPUT POSITIVE AND GATES



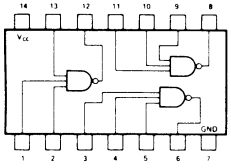
7409 QUAD 2-INPUT AND GATE WITH OPEN COLLECTOR OUTPUTS



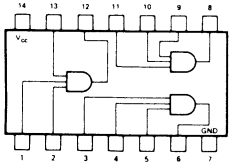
DESCRIPTION

The 54/7409 Quad 2-Input AND Gate with open collector outputs provides the capability of expanding AND logic functions.

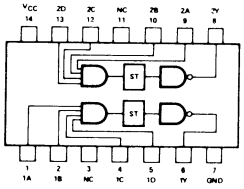
7410 TRIPLE 3-INPUT POSITIVE NAND GATE



7411 TRIPLE 3-INPUT POSITIVE AND GATE



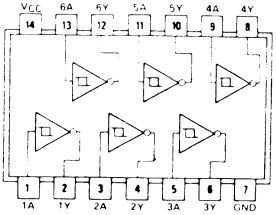
7413 DUAL NAND SCHMITT TRIGGER



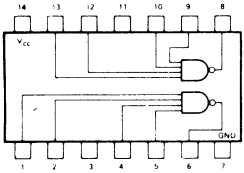
DESCRIPTION

The 5413 and 7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800mV.

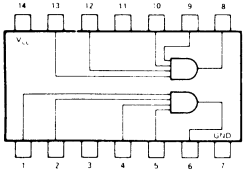
7414 HEX SCHMITT TRIGGER



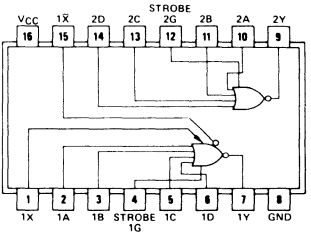
7420 DUAL 4-INPUT POSITIVE NAND GATE



7421 DUAL 4-INPUT POSITIVE AND GATE



7423 EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE



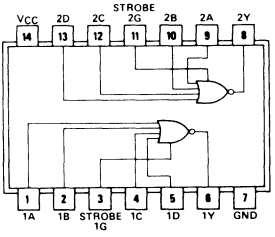
positive logic:

$1Y = \overline{1G(1A+1B+1C+1D)+X}$

$2Y = \overline{2G(2A+2B+2C+2D)}$

X = output of SN5460/SN7460

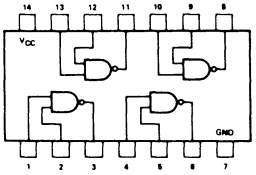
7425 DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE



positive logic:

$Y = \overline{G(A+B+C+D)}$

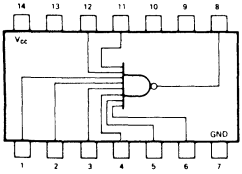
7426 QUAD 2-INPUT HIGH VOLTAGE NAND GATE



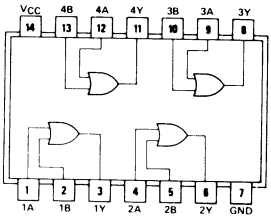
DESCRIPTION

The 54/7426 Quad 2-Input NAND Gate features standard TTL inputs with high voltage (15 volts) open collector outputs for interface with MOS, lamps or relays.

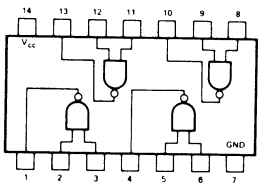
7430 8-INPUT POSITIVE NAND GATE



7432 QUADRUPLE 2-INPUT POSITIVE OR GATES



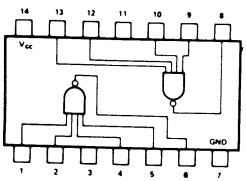
7437
7438 QUADRUPLE 2-INPUT POSITIVE NAND BUFFER



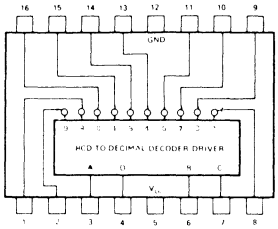
The S5437/N7437 is a NAND Gate (output low only **when** all inputs are high) the same as N7400 except that it will drive 3 times as many loads. The S5438/N7438 and S5439/N7439 are also NAND Gates but have open-collectors similar to N7403.

The S5437/N7437, S5438/N7438 and S5439/N7439 contain four 2-input NAND gates in a package with a guaranteed fan-out of 30-series 54/74 loads in both the logical "1" (1.2mA), and logical "0" (48mA) states. The S5438/N7438 and S5439/N7439 have an open collector output for "WIRE-AND" applications but still retain the high sink current capability of the S5437/N7437.

7440 DUAL 4-INPUT POSITIVE NAND BUFFER



7441 BCD-TO-DECIMAL DECODER/DRIVER



DESCRIPTION

The N7441B Nixie† Decoder/Driver is a one-out-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes.

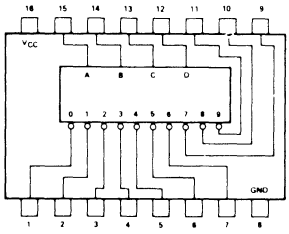
It may also be utilized in driving relays or other high voltage interface circuitry. The element is designed using TTL techniques and is therefore completely compatible with DTL and TTL elements.

The specially designed output drivers provide the necessary stable output state. There are no input codes where all outputs are "off" or where more than one output can be turned "on".

INPUT				OUTPUT
D	C	B	A	ON†
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

† All other inputs are off.

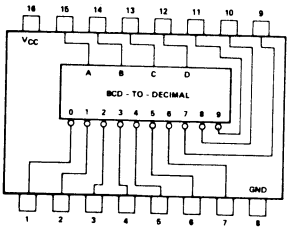
7442 BCD-TO-DECIMAL DECODER



D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

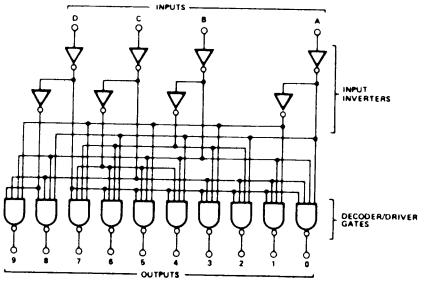
7445
74145 BCD-TO-DECIMAL DECODER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS



DESCRIPTION

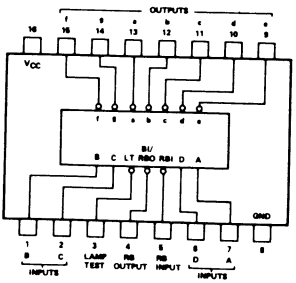
The 54/7445 and 54/74145 BCD-to-Decimal Decoder/Driver is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The 54/7445 minimum output breakdown is 30 volts and the 54/74145 minimum output breakdown is 15 volts.

LOGIC DIAGRAM



NOTE: 1. These voltage values are with respect to network ground terminal.

7446
7447 BCD-TO-SEVEN SEGMENT DECODER/DRIVER


OUTPUTS
f g a b c d e
16 15 14 13 12 11 10 9
Vcc
f g a b c d e
BI/ RBO
B C LT RBO RBI D A
GND
1 2 3 4 5 6 7 8
B C LAMP TEST BI/RBO OUTPUT RB INPUT D A
INPUTS
INPUTS

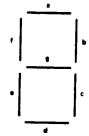
DESCRIPTION

The 7446 and 7447 BCD-to-Seven Segment Decoder/Driver are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

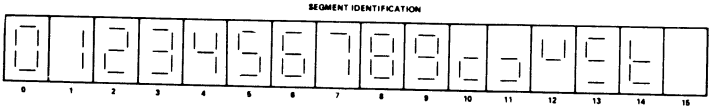
Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

The 7446 and 7447 provide bare collector output transistors for directly driving lamps. The output transistor breakdown of the 7446 is 30 volts and the 7447 is 15 volts.

1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

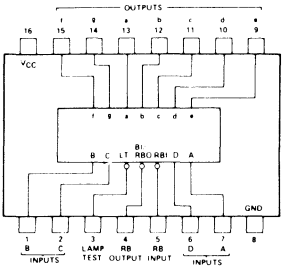


SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

7448 BCD-TO-SEVEN SEGMENT DECODER/DRIVER



DESCRIPTION

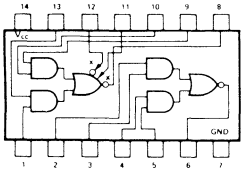
The 7448 BCD-to-Seven Segment Decoder/Driver is a TTL monolithic device consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

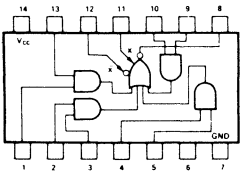
The 7448 has resistor pull up on the outputs to provide source current to drive interface elements.

	INPUTS						OUTPUTS							
FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	x	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	x	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	x	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	x	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	x	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	x	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	x	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	x	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	x	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	x	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	x	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	x	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	x	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	x	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	x	1	1	1	1	1	0	0	0	0	0	0	0	
BI	x	x	x	x	x	x	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	x	x	x	x	x	1	1	1	1	1	1	1	1	4

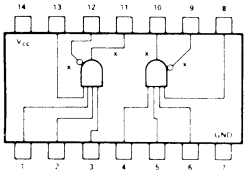
7450 7451 EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



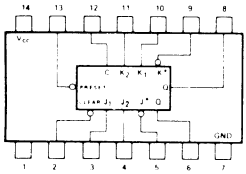
7453 7454 4-WIDE 2-INPUT AND-OR-INVERT GATE



7460 DUAL 4-INPUT EXPANDER



7470 J-K FLIP-FLOP



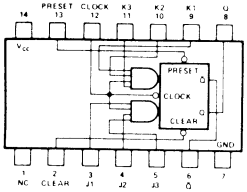
DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

7472 J-K MASTER-SLAVE FLIP-FLOP



LOGIC

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

DESCRIPTION

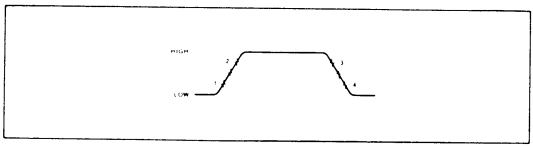
These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

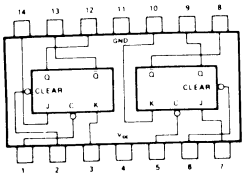
NOTES:

1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. **NC = No Internal Connection.**

CLOCK WAVEFORM



7473 DUAL J-K MASTER-SLAVE FLIP-FLOP

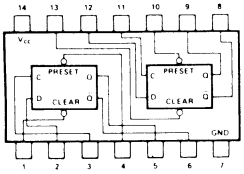


DESCRIPTION

The S5473/N7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



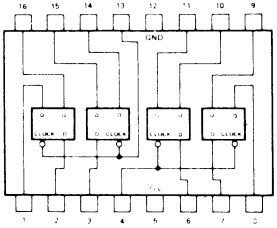
DESCRIPTION

The S5474/N7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

POSITIVE LOGIC – Low input to preset sets Q to logical 1 Low input to clear sets Q to logical 0; Preset and clear are independent of clock

7475 QUADRUPLE BISTABLE LATCH



DESCRIPTION

The S5475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

TRUTH TABLE

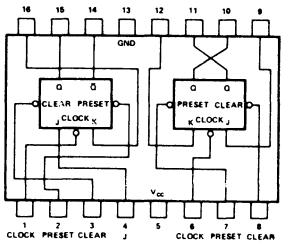
LOGIC

(Each Latch)		
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

NOTES:

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse
3. These voltages are with respect to network ground terminal.

7476 DUAL J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

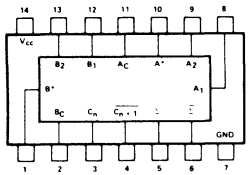


DESCRIPTION

The S5476B/N7476B J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

7480 GATED FULL ADDER



DESCRIPTION

The S5480/N7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

TRUTH TABLE (See Notes 1,2, and 3)

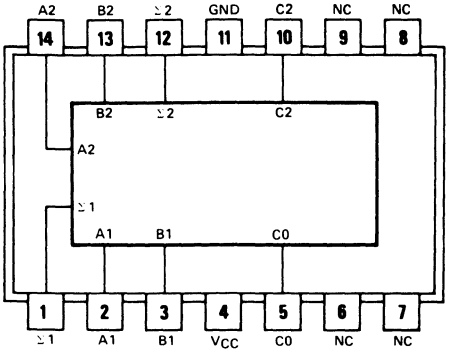
LOGIC

C_n	B	A	C_{n+1}	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES:

1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$, $B^* = \overline{B_1 \cdot B_2}$.
2. When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively, must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively, must be open or used to perform Dot-OR logic.
4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

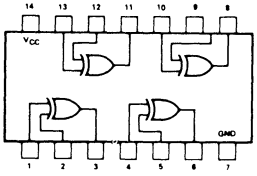
7482 2 BIT BINARY FULL ADDER



description

These full adders perform the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, these circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) and are compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

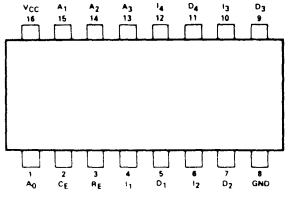
7486 QUAD 2-INPUT EXCLUSIVE OR GATE



DESCRIPTION

The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function $\overline{A}B + A\overline{B}$ at the output.

7489 64-BIT READ/WRITE MEMORY (RAM)



DESCRIPTION

The 7489 is a TTL 64-Bit Read-Write Random Access Memor organized as 16-words of 4 bits each. The 7489 is ideally suited fc application in scratch pads and high speed buffer memories.

Words are selected through a 4-input binary decoder when the ch select input (CE) is at logic "0". Data is written into the memor when Read Enable (RE) is at logic "0" and read from the memor when RE is at logic "1".

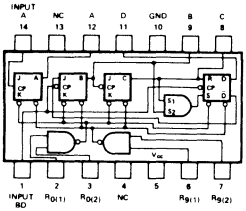
RE	$\overline{CE}$ (Chip Enable)	MODE	OUTPUTS
0	0	Write	"1"
1	0	Read	Information
X	1	Chip Disable	"1"

X = Either State

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
PUSH DOWN STACKS (First in–first out)
CONTROL STORE

7490 DECADE COUNTER



DESCRIPTION

The S5490/N7490 is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical "0" or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional "0" reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

The 5490/7490 is completely compatible with Series 54 and Series 74 logic familes. Average power dissipation is 160mW.

BCD COUNT SEQUENCE (See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

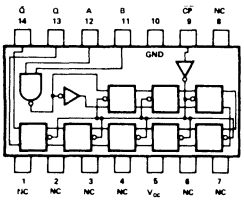
NOTES:
1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted

7491 8-BIT SHIFT REGISTER

LOGIC

t_n A	B	t_{n+8} Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+8} = bit time after 8 clock pulse.



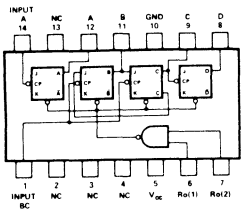
DESCRIPTION

The S5491/N7491 is a monolithic serial-in, serial-out 8-bit shift register utilizing high-speed transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes the S5491/N7491 to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the S5470/N7470 flip-flop and the S5474/N7474 dual D-type flip-flop.

7492 DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)



COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

COUNT	OUTPUT			
	D	C	B	A
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

DESCRIPTION

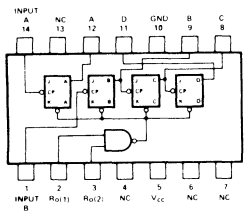
The S5492/N7492 is a high-speed monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flops outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous division of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency division of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

NOTES:
1. Output A connected to input B
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

7493 4-BIT BINARY COUNTER



COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

DESCRIPTION

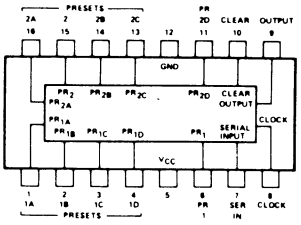
The S5493/N7493 is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

7494 4-BIT SHIFT REGISTER (PARALLEL-IN, SERIAL-OUT)



DESCRIPTION

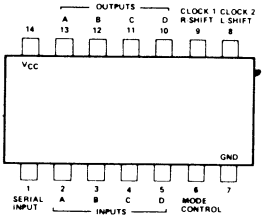
This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The output of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

7495 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER



DESCRIPTION

The 54/7495 is a monolithic universal 4-Bit Shift Register designed with standard TTL techniques. The circuit layout consists of 4 R-S master-slave flip-flops, 4 AND-OR-INVERT gates, and 6 inverters configured to form a versatile register which will perform right-shift, left-shift, or parallel-in, parallel-out operations depending on the logical input level to the mode control.

- Right-shift operations are performed when a logical 0 level is applied to the mode control. Serial data is entered at the serial input D_S and shifted one position right on each clock 1 pulse. In this mode, clock 2 and parallel inputs D_A thru D_D are inhibited.

- Parallel-in, parallel-out operations are performed when a logical 1 level is applied to the mode control. Parallel data is entered at parallel inputs D_A thru D_D and is transferred to the data outputs A_0 thru D_0 on each clock 2 pulse. In this mode, shift-left operations may be implemented by externally tying the output of each flip-flop to the parallel input of the previous flip-flop (D_0 to D_C and etc.), with serial data entry at input D_D.

Information must be present at the R-S inputs prior to clocking and transfer of data occurs on the falling edge of the clock pulse.

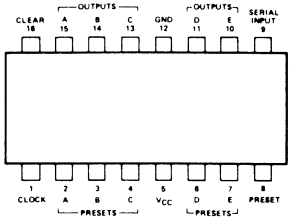
LOGIC

(Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES:
1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

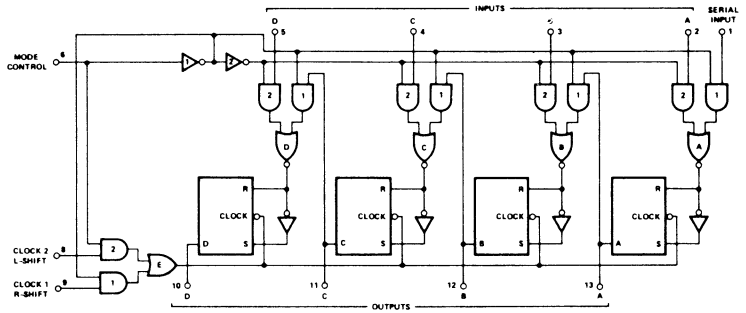
NC – No internal connection.

7496 5-BIT SHIFT REGISTER

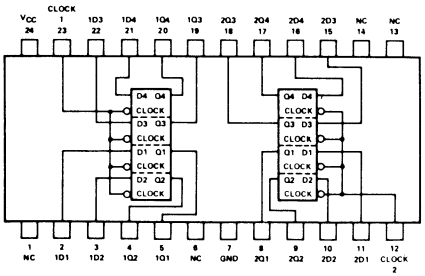


DESCRIPTION

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator unjts. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.



74100 4-BIT BISTABLE LATCH

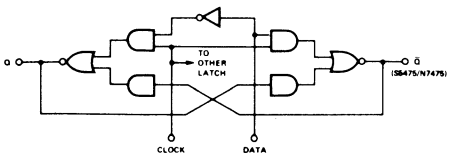


DESCRIPTION

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

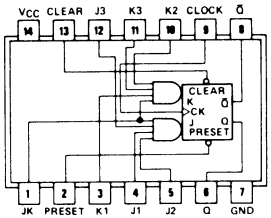


Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

74104 GATED J K MASTER SLAVE FLIP FLOP

FUNCTION TABLE

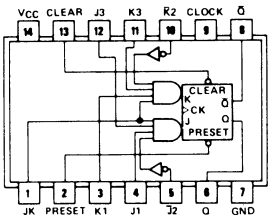
INPUTS						OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	JK	Q	$\bar{Q}$
L	H	X	X	X	X	H	L
H	L	X	X	X	X	L	H
L	L	X	X	X	X	H*	H*
H	H	⊔	X	X	L	Q_0	Q_0
H	H	⊔	L	L	X	Q_0	$\bar{Q}_0$
H	H	⊔	H	L	H	H	L
H	H	⊔	L	H	H	L	H
H	H	⊔	H	H	H	TOGGLE	



74105 GATED J K MASTER SLAVE FLIP FLOP

FUNCTION TABLE

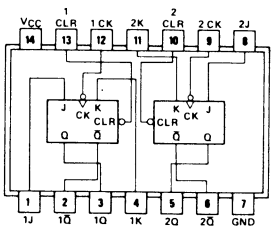
INPUTS						OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	JK	Q	$\bar{Q}$
L	H	X	X	X	X	H	L
H	L	X	X	X	X	L	H
L	L	X	X	X	X	H*	H*
H	H	⊔	X	X	L	Q_0	$\bar{Q}_0$
H	H	⊔	L	L	X	Q_0	$\bar{Q}_0$
H	H	⊔	H	L	H	H	L
H	H	⊔	L	H	H	L	H
H	H	⊔	H	H	H	TOGGLE	



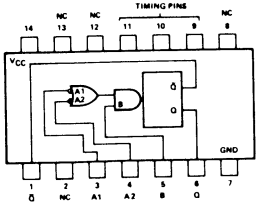
74107 DUAL J K MASTER SLAVE FLIP FLOP

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	



74121 MONOSTABLE MULTIVIBRATOR



DESCRIPTION

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

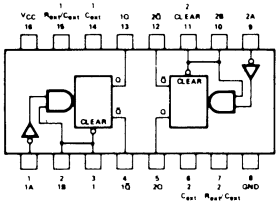
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T - 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin (9) to pin (14)
5. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.
7. t_n = time before input transition.
8. t_{n+1} = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

74122
74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR



DESCRIPTION

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. N74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with N74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000pF$, the output pulse width (t_w) is defined as:

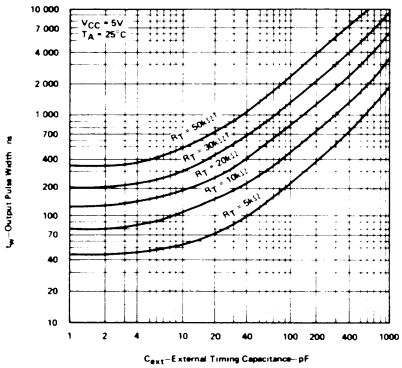
$$t_w = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

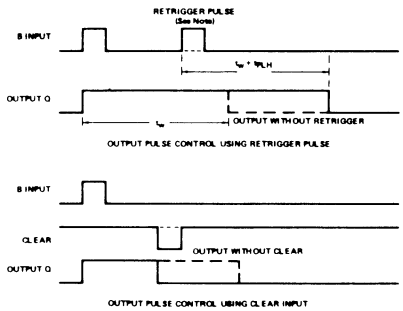
where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leq 1000pF$, see Figure B.

OUTPUT PULSE WIDTH VS EXTERNAL TIMING CAPACITANCE





N74122

INPUTS				OUTPUTS	
A_1	A_2	B_1	B_2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
	H	H	H	⎍	⎎

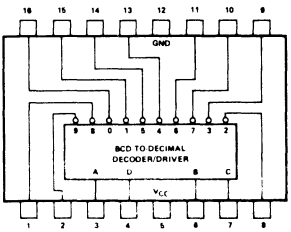
NOTES:
A. H = high level (steady-state), L = low level (steady-state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = No internal connection.
C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

S54123,N74123

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

74141 BCD-TO-DECIMAL DECODER/DRIVER WITH BLANKING



DESCRIPTION

The N74141 is a BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the N74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The then high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

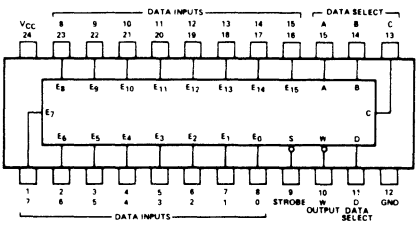
Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The N74141 is characterized for operation over the temperature range of 0°C to 70°C.

INPUT				OUTPUT
D	C	B	A	ON*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level

*All other outputs are off

74150


DATA INPUTS
DATA SELECT
V_{CC} 24
8 9 10 11 12 13 14 15
23 22 21 20 19 18 17 16
A B C
15 14 13
E_8 E_9 E_{10} E_{11} E_{12} E_{13} E_{14} E_{15} A B
E_7 C
E_6 E_5 E_4 E_3 E_2 E_1 E_0 S W D
1 2 3 4 5 6 7 8 9 10 11 12
7 6 5 4 3 2 1 0
STROBE W OUTPUT D DATA SELECT GND
DATA INPUTS

DESCRIPTION

The 54/74150 is a one-of-sixteen data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

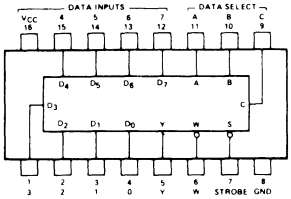
The S54150/N74150 is provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

This data selector/multiplexer is fully compatible for use with other TTL or DTL circuit. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

S54150/N74150 – 200 milliwatts.

INPUTS																				OUTPUT
D	C	B	A	STROBE	e_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1

74151 8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

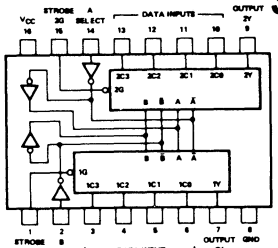


DESCRIPTION

The 54/74151 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line. Both true and complement outputs are available.

INPUTS											OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

74153 DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER



DESCRIPTION

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

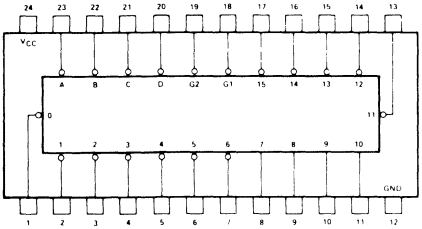
These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections. H = high level, L = low level, X = irrelevant.

74154 4-LINE TO 16 LINE DECODER/DEMULTIPLEXER



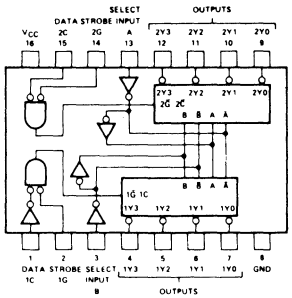
DESCRIPTION

The 54/74154 decodes 4 binary-coded inputs to one of 16 mutually exclusive outputs when each of the two strobe inputs are low. The demultiplexing function is achieved by using the 4 input lines for output addressing and data from one strobe input while the other strobe input is held low.

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High, L = Low, X = Irrelevant

74155 74156 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

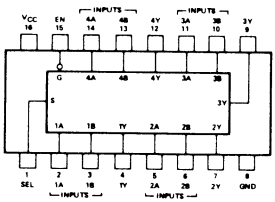


DESCRIPTION

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired.

The S54155/N74155 circuits, with totem pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The S54156/N74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

74157 QUADRUPLE 2-INPUT DATA
74158 SELECTOR/MULTIPLEXER



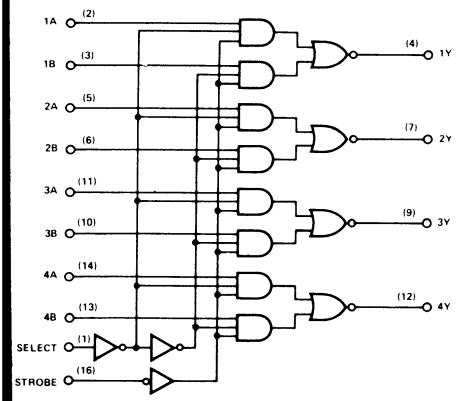
DESCRIPTION

The S54157/N74157 and S54158/N74158 are identical with the exception of the S54158/N74158 being inverted. These devices are logical implementations of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The devices provide the ability, in one package, to select four bits of either data or control from two sources. By proper manipulation of the inputs, it can generate four functions of two variables with one variable common. Thus any number of random topic elements used to generate unusual truth tables can be replaced. All outputs are low when disabled (enable high). Both inputs and outputs are buffered.

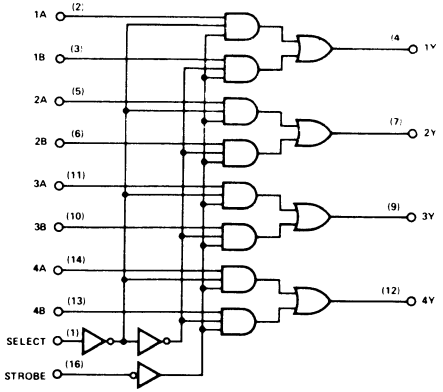
TRUTH TABLE

INPUTS			OUTPUT
STROBE	SELECT	A B	Y
H	X	X X	H
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

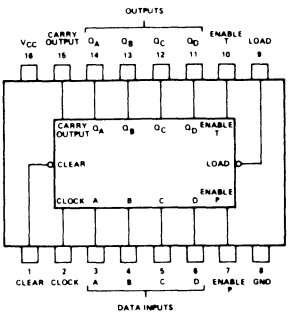
LOGIC DIAGRAM
S54/N74157



LOGIC DIAGRAM
S54/N74158



74160
74161
74162
74163
SYNCHRONOUS 4-BIT COUNTER

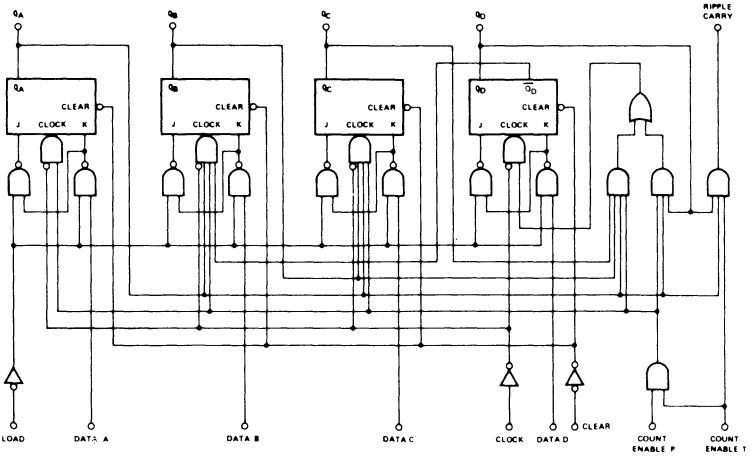


DESCRIPTION

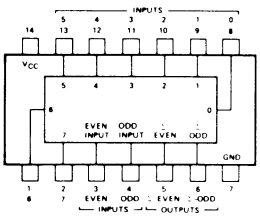
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The S54160, S54162, N74160, and N74162 are decade counters and the S54161, S54163, N74161, and N74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

S54160/N74160 SYNCHRONOUS DECADE COUNTERS

(S54162/N74162 synchronous decade counters are similar; however the clear is synchronous as shown for the S54163/N74163 binary counters).



74180 8-BIT ODD/EVEN PARITY GENERATOR/CHECKER



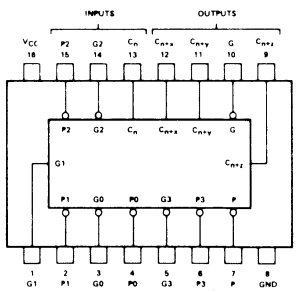
DESCRIPTION

The 54/74180 8-Bit Odd/Even Parity Generator/Checker is a TTL monolithic array featuring gating logic arranged to generate or check odd or even parity.

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

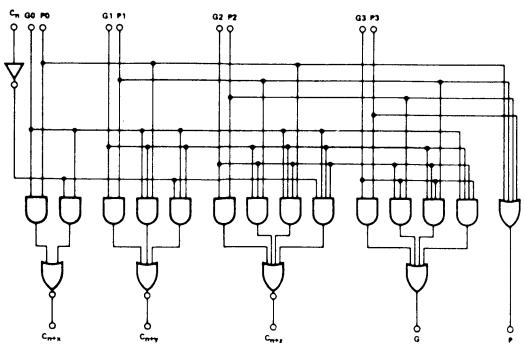
74182 LOOK-AHEAD CARRY GENERATOR


INPUTS
OUTPUTS
VCC 16 P2 15 G2 14 Cn 13 Cn+x 12 Cn+y 11 G 10 Cn+z 9
P2 G2 Cn Cn+x Cn+y G
G1
Cn+z
P1 G0 P0 G3 P3 P
1 G1 2 P1 3 G0 4 P0 5 G3 6 P3 7 P 8 GND
OUTPUT
INPUTS

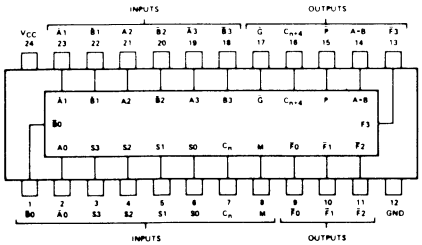
DESCRIPTION

The S54182, N74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanoseconds delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

The S54182 or N74182, when used in conjunction with the S54181 or N74181 arithmetic logic unit (ALU), provides full high-speed carry look-ahead capability for up to n-bit words. Each S54182/ N74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. Applications data for the S54181/N74181 illustrates cascading of S54182/N74182 circuits to perform multi-level look-ahead.



74181 HIGH-SPEED ARITHMETIC LOGIC



SELECTION $S_3 S_2 S_1 S_0$	M = H LOGIC FUNCTIONS	ACTIVE HIGH DATA M = L; ARITHMETIC OPERATIONS C_n = 0	C_n = 1
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $A\overline{B}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A + B}$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A ⊕ B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + B) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

SELECTION $S_3 S_2 S_1 S_0$	M = H LOGIC FUNCTIONS	ACTIVE LOW DATA M = L; ARITHMETIC OPERATIONS C_n = 0	C_n = 1
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A ⊕ B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

	Input C_n	Output C_{n+4}	Indicates
Active-high Data	H	H	A < B
	L	H	A = B
	H	L	A ≠ B
	L	L	A > B
Active-low Data	L	L	A < B
	H	L	A = B
	L	H	A ≠ B
	H	H	A > B

DESCRIPTION

The 54181 and 74181 are high-speed arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the 54181/74181 for fast, simultaneous carry generation with a group carry propagate (P) and carry generate (G) for the 4 bits in the package. When used in conjunction with the 54182 or 74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the 54181/74181 is 24 nanoseconds for 4 bits. When expanding to 16-bit addition with the 54182/74182, only 13 nanoseconds, further delay is added so that the total addition time is 35 nanoseconds, or 2.2 nanoseconds per bit. One 54182/74182 is needed for every 16 bits (four 54181/74181 circuits).

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

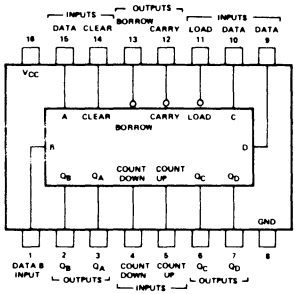
Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1 which requires an end-around or forced carry to provide A−B.

The 54181/74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The 54181/74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR and OR functions.

The 54181/74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

74192 SYNCHRONOUS DECADE UP/DOWN COUNTER WITH PRESET INPUTS



DESCRIPTION

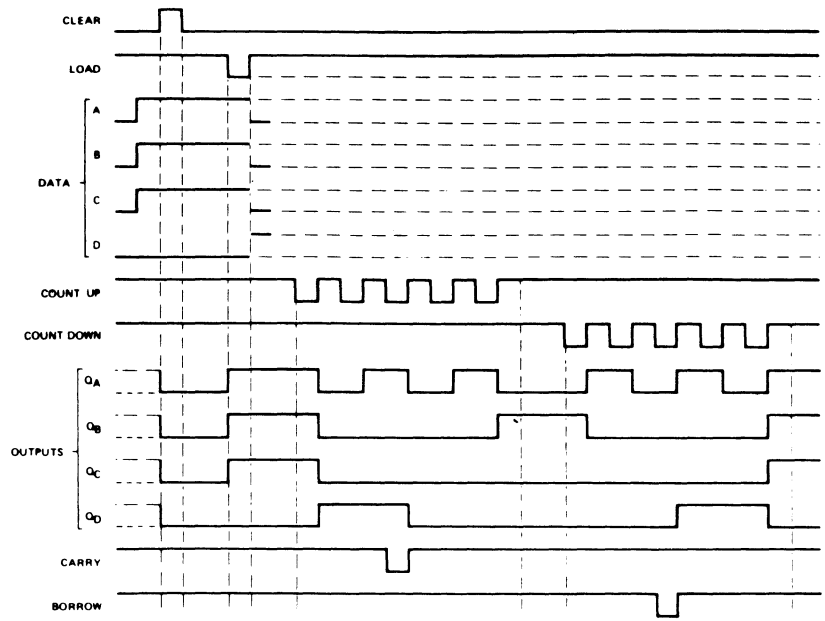
This is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. The S54192 and N74192 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

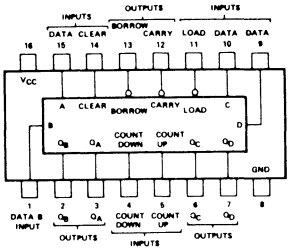
These counters are fully programmable; that is, the outputs may be present to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.



74193 SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH PRESET INPUTS



DESCRIPTION

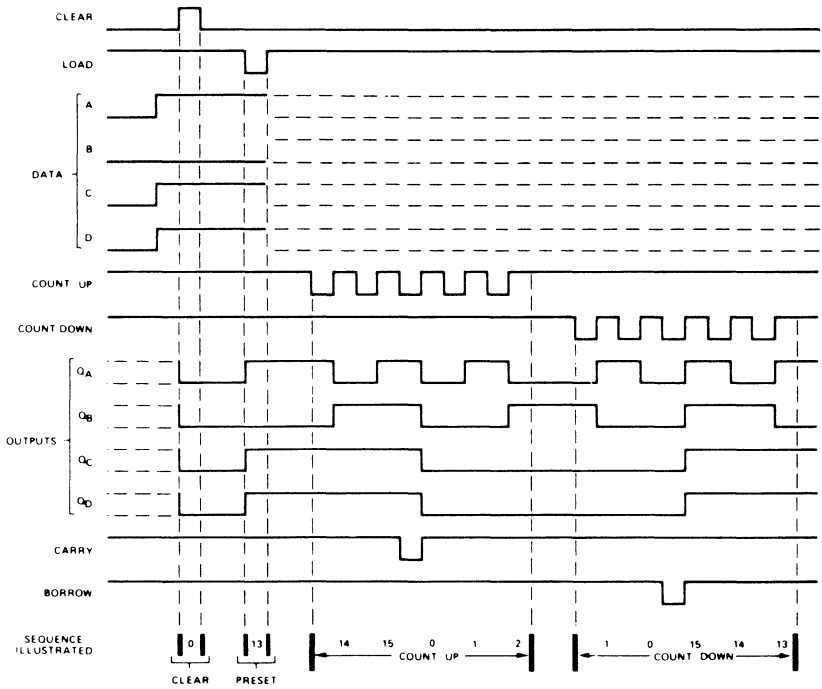
The S54193 and N74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

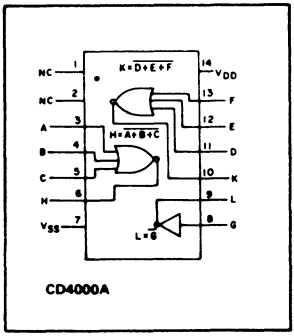
The oututs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simplv modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.





CD4000A

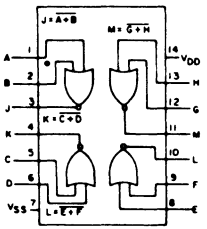
COS/MOS NOR Gates (Positive Logic)

Special Features

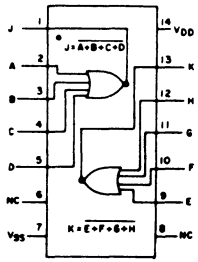
- Medium speed operation..... $t_{PHL} = t_{PLH} = 25$ ns (typ.) at $C_L = 15$ pF
- Low "high"- and "low"-level output impedance..... 500Ω and 200Ω (typ), respectively at $V_{DD} - V_{SS} = 10$ V

Dual 3 Input plus Inverter	CD4000AD, CD4000AE, CD4000AF, CD4000AK
Quad 2 Input	CD4001AD, CD4001AE, CD4001AF, CD4001AK
Dual 4 Input	CD4002AD, CD4002AE, CD4002AF, CD4002AK
Triple 3 Input	CD4025AD, CD4025AE, CD4025AF, CD4025AK

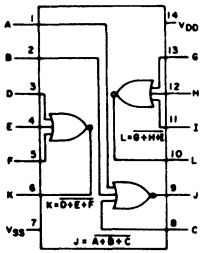
The combination of these devices and the RCA NAND positive logic gate types CD4011A, CD4012A, and CD4023A can account for appreciable package-count savings in various logic function configurations.



CD4001A

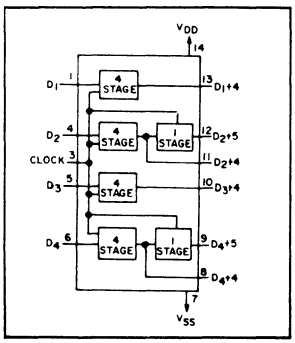


CD4002A



CD4025A

CD4006AD, CD4006AF
CD4006AE, CD4006AK



COS/MOS 18-Stage Static Shift Register

Special Features

- Fully static operation
- Up to 5 MHz shifting rates
- Permanent register storage with clock line "high" or "low" — — — no information recirculation required

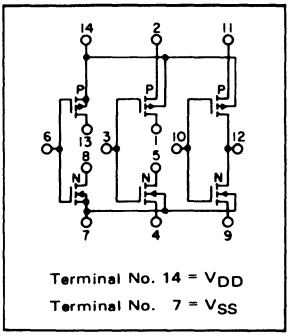
Applications

- Serial shift registers
- Time delay circuits
- Frequency division

CD4006A types are comprised of 4 separate "shift register" sections; two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent "single rail" data path.

A common clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the clock.

Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.



Terminal No. 14 = V_{DD}
Terminal No. 7 = V_{SS}

COS/MOS Dual Complementary Pair Plus Inverter

Special Features

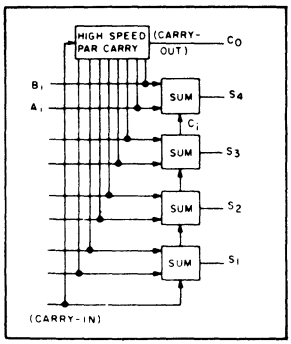
- **Medium speed operation. . . $t_{PHL} = t_{PLH}$ = 20 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low"-output impedance. . . . . 500 Ω (typ.) at $V_{DD} - V_{SS}$ = 10 V**

Applications

- **Extremely high-input impedance amplifiers; inverters, shapers, linear amplifiers, threshold detector**

CD4007A types are comprised of three N-Channel and three P-Channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits shown in Fig.4.1.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed. For proper operation $V_{SS} \leq V_I \leq V_{DD}$ must be satisfied.



COS/MOS Four-Bit Full Adder

With Parallel Carry Out

Special Features

- **MSI complexity on a single chip. . . . . 4 Sum Outputs plus parallel Carry-Output**
- **High speed operation. . . . . Carry-In to Carry-Out delay, t_{PHL}, t_{PLH} = 45 ns at C_L = 15 pF**

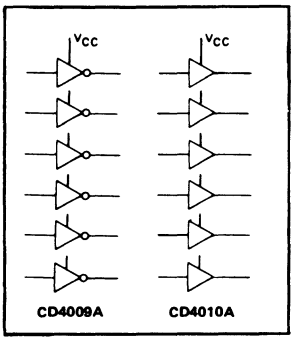
Applications

- **Binary addition/arithmetic units**

TRUTH TABLE

A_i	B_i	C_i	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008A outputs include the four sum bits, S_1 and S_4, in addition to the high-speed "parallel-cary-out" which may be utilized at a succeeding CD4008A section.



COS/MOS Hex Buffers/Converters

Inverting Type: CD4009AD, CD4009AE, CD4009AK
Non-Inverting Type: CD4010AD, CD4010AE, CD4010AK

Special Features (Each Buffer)

- **High current sinking capability..... 8 mA (min.) at V_{OL} = 0.5 V and V_{DD} = + 10 V**

Applications

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS logic-level converter**
- **COS/MOS current "sink" or "source" driver**
- **Multiplexer—1 to 6 or 6 to 1**

CAUTION:
V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS THAN V_{DD}. FOR 10.5- TO 15-VOLT SUPPLIES, C_{LOAD} MUST BE EQUAL TO OR LESS THAN 5000 pF.

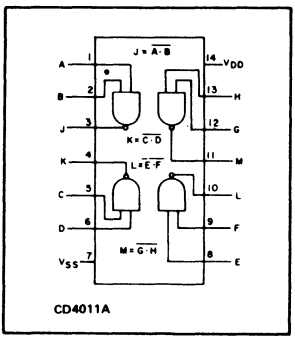
CD4009A types may be used as a hex COS/MOS inverter, a COS/MOS to DTL or TTL logic-level converter, or a COS/MOS current driver.

The CD4049A and CD4050A are preferred Hex Buffer replacements for the CD4009A and CD4010A, respectively, in all applications except multiplexers.

CD4010A types may be used as a COS/MOS to DTL or TTL hex converter or a COS/MOS current driver.

Conversion ranges are from COS/MOS logic operating at +3 V to +15 V supply levels to DTL or TTL logic operating at +3 V to +6 V supply levels. Conversion to logic output levels greater than +6 V is permitted providing V_{CC}(DTL/TTL) ≤ V_{DD}(COS/MOS).

CD4011A, CD4012A, CD4023A



CD4011A

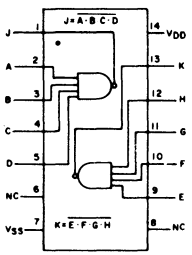
COS/MOS NAND Gates
(Positive Logic)

Quad 2 Input • • • CD4011AD, CD4011AE, CD4011AF, CD4011AK
Dual 4 Input • • • CD4012AD, CD4012AE, CD4012AF, CD4012AK
Triple 3 Input • • • CD4023AD, CD4023AE, CD4023AF, CD4023AK

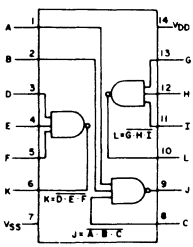
Special Features

- **Medium speed operation..... t_{PHL} = t_{PLH} = 25 ns (typ.) at C_L = 15 pF**
- **Low "high"- and "low"-level output impedance..... 400 and 800Ω (typ.) respectively at $V_{DD} - V_{SS}$ = 10 V**

The combination of these devices and the RCA NOR positive logic gate types CD4000A, CD4001A, CD4002A, and CD4025A can account for appreciable package-count savings in various logic function configurations.

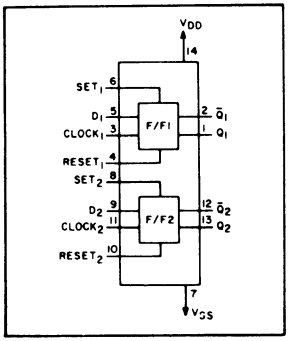


CD4012A



CD4023A

CD4013AD, CD4013AF
CD4013AE, CD4013AK



Dual 'D'-Type Flip-Flop

With Set-Reset Capability

Special Features

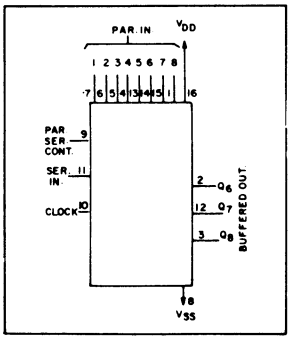
- **Static flip-flop operation..... retains state indefinitely with clock level either "high" or "low"**
- **Medium speed operation..... 10 MHz (typ.) clock toggle rate at $V_{DD} - V_{SS} = 10$ V**
- **Low "high"- and "low" output impedance..... 400Ω and 200Ω, respectively at $V_{DD} - V_{SS} = 10$ V**

Applications

- **Registers, counters, control circuits**

CD4013A types consist of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and, by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

CD4014AD, CD4014AF
CD4014AE, CD4014AK



COS/MOS 8-Stage Static Shift Register

SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT

Special Features

- **Medium speed operation..... 5 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **MSI complexity on a single chip..... 8 master-slave flip-flops plus output buffering and control gating**

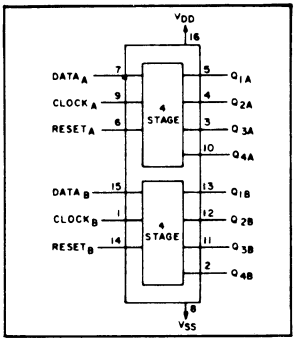
Applications

- **Synchronous parallel input/serial output data queueing**
- **Parallel to serial data conversion**
- **General purpose register**

CD4014A types are 8-stage parallel-input/serial output registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7.

Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the Parallel/Serial Control input. When the Parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD4014A packages is permitted.

CD4015AD, CD4015AF
CD4015AE, CD4015AK



COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

Special Features

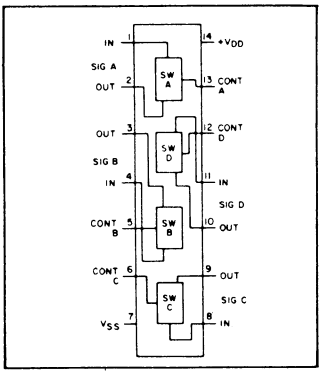
- **Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **MSI complexity on a single chip. . . . . 8 master-slave flip-flops plus output buffering**

Applications

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General purpose register**

RCA CD4015A types consist of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master- slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A s is possible.

CD4016AD, CD4016AF
CD4016AE, CD4016AK



COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

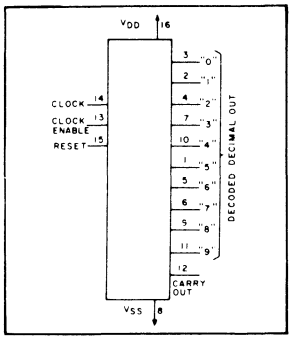
Special Features

- **Wide range of digital and analog signal levels — Digital or analog signal to 15 V peak Analog signal ±7.5 V peak**
- **Low "ON" resistance— 300 Ω typ. over 15 V_{p-p} signal input range, for $V_{DD} - V_{SS} = 15$ V**
- **Matched switch characteristics — 40Ω typ. difference between R_{ON} values at a fixed bias point over 15 V_{p-p} signal input range $V_{DD} - V_{SS} = 15$ V**
- **High "On/Off" output voltage ratio — 65 dB typ. @ $f_{is} = 10$ kHz, $R_L = 10$ kΩ**
- **High degree of linearity — < 0.5% distortion typ. @ $f_{is} = 1$kHz, $V_{is} = 5\ V_{p-p}$, $V_{DD} - V_{SS} \geq 10$V, $R_L = 10$kΩ.**

Applications

- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/Multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**
- **Extremely low "OFF" switch leakage resulting in very low offset current and high effective "OFF" resistance — 10 pA typ. @ $V_{DD} - V_{SS} = 10$ V, $T_A = 25°C$**
- **Extremely high control input impedance (control circuit isolated from signal circuit) — $10^{12}\Omega$ typ.**
- **Low crosstalk between switches — −50 dB typ. @ $f_{is} = 0.9$ MHz, $R_L = 1$ kΩ**
- **Matched control-input to signal-output capacitances — Reduces output signal transients**
- **Transmits frequencies up to 10 MHz**

CD4017AD, CD4017AF
CD4017AE, CD4017AK



COS/MOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

Special Features

- Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- MSI complexity on a single chip. . . . . decade counter plus 10 decoded outputs

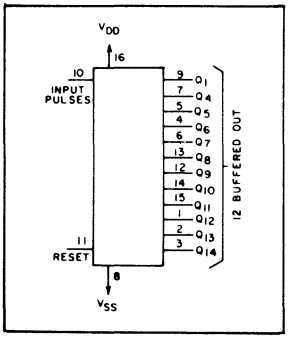
Applications

- Decade counter/decimal decode display applications
- Frequency division
- Counter control/timers
- Divide by N counting
  N = 2 – 10 with one CD4017A and one CD4001A
  N > 10 with multiple CD4017A's
- For further application information, see ST4166 "COS/MOS MSI Counter and Register Design & Applications"

CD4017A types consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a "Clock", a "Reset", and a "Clock Enable" signal.

The decade counter is advanced one count at the positive clock signal transition if the clock enable signal is "low". Counter advancement via the clock line is inhibited when the clock enable signal is "high". A "high" reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally "low" and go "high" only at their respective decimal time slot. Each decoded output remains "high" for one full clock cycle. A carry-out (C_{OUT}) signal completes one cycle every 10 clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

CD4020AD, CD4020AF
CD4020AE, CD4020AK



COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider

Special Features

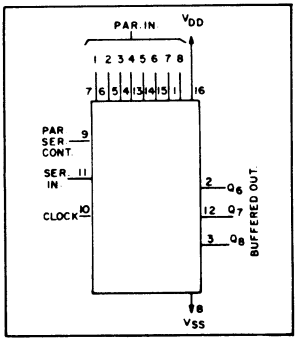
- Medium speed operation. . . . . 7 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Low "high"- and "low"-level output impedance. . . . . 1000Ω (typ.) at $V_{DD} - V_{SS} = 10$ V
- MSI complexity on a single chip. . . . . 14 fully static, master-slave stages
- COS/MOS gate-input loading at both Reset and Input-pulse lines

CD4020A types consist of a pulse input shaping circuit, reset line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeroes" state by a high level on the reset inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each input pulse.

Applications

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

CD4021AD, CD4021AF
CD4021AE, CD4021AK



COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output, Synchronous Serial Input/Serial Output

Special Features

- Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input
- Individual "jam" inputs to each register stage
- Master-slave flip-flop register stages
- Fully static operation. . . . . DC to 5 MHz

CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages.

When the parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse.

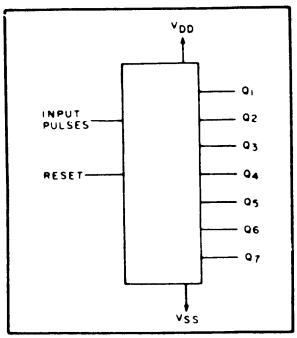
Applications

- Asynchronous parallel input/serial output data queueing
- Parallel to serial data conversion
- General purpose register

When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

Register expansion is possible using additional CD4021A packages.

CD4024AD,CD4024AE,CD4024AF
CD4024AK,CD4024AT



COS/MOS 7-Stage Binary Counter

With Buffered Reset

Special Features:

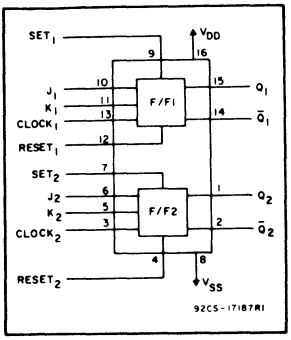
- Medium speed operation. . . . . 7 MHz (typ.) input pulse rate at $V_{DD}-V_{SS}$ = 10 V
- Low "high" and "low" level output impedance. . . . .700Ω and 500Ω (typ.), respectively at $V_{DD}-V_{SS}$ = 10 V
- Logic block complexity on a single chip. . . . . .each output accessible and resettable
- Static counter operation — counter retains state indefinitely with input pulse level "low" or "high"
- COS/MOS gate input loading on both reset and input-pulse lines

The CD4024A types consist of an input pulse shaping circuit, reset line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- D/A counter and switch on one chip

* Formerly developmental type TA5385C.



COS/MOS Dual J-K Master-Slave Flip-Flop

With Set/Reset Capability

Special Features:

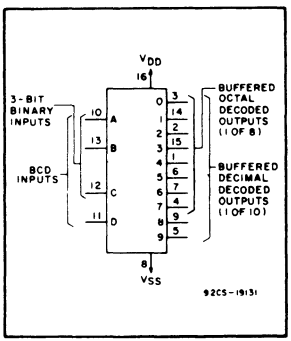
- Static flip-flop operation. . . . . .retains state indefinitely with clock level either "high" or "low"
- Medium speed operation. . . . . .8 MHz (typ.) clock toggle rate at $V_{DD}-V_{SS}$ = 10 V
- Low "high"-and "low" output impedance. . . . . .700Ω and 300Ω, respectively, at $V_{DD}-V_{SS}$ = 10 V

Applications:

- Registers, counters, control circuits

RCA CD4027A▲ is a single monolithic chip integrated circuit containing two identical complementary-symmetry "J-K" master-slave flip-flops. Each flip-flop has provisions for individual "J", "K", "Set", "Reset", and "Clock" input signals. Buffered "Q" and "Q̄" signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA CD4013A dual "D"-type flip-flop.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the "J" and "K" inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the "clock" pulse. Set and reset functions are independent of the clock and are initiated when a "high" level signal is present at either the "Set" or "Reset" input.



COS/MOS BCD-to-Decimal Decoder

Special Features:

- BCD to decimal decoding or binary to octal decoding
- High decoded output drive capability. . . . . .8 mA (typ.) sink or source
- "Positive logic" inputs and outputs. . . . . .decoded outputs go "high" on selection
- Medium speed operation. . . . . t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V

Applications:

- Code conversion
- Indicator-tube decoder
- Address decoding—memory selection control

RCA CD4028A▲ types are BCD to decimal or binary to octal decoders consisting of pulse shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D results in a "high" level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A "high"-level signal at the D input inhibits octal decoding and causes inputs 0 through 7 to go "low". If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

All inputs and outputs are protected against electrostatic effects.

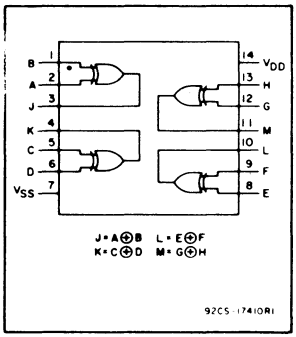
▲ Formerly developmental type TA5873.

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

CD4030AD, CD4030AF
CD4030AE, CD4030AK



COS/MOS Quad Exclusive-OR Gate

(Positive Logic)

Special Features:

- **Medium speed operation. . . . . $t_{PHL} = t_{PLH}$ = 40 ns (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V**
- **Low output impedance. . . . . 500Ω (typ.) @ $V_{DD}-V_{SS}$ = 10 V**

Applications:

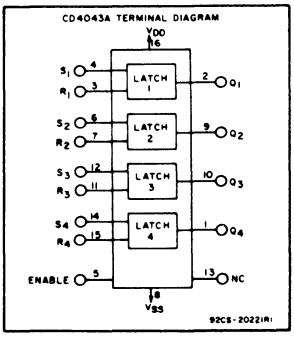
- **Even and odd-parity generators and checkers**
- **Logical comparators**
- **Adders/subtractors**
- **General logic functions**

RCA CD4030A▲ types each contains four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four N-channel and four P-channel enhancement-type transistors.

All inputs and outputs are protected against electrostatic effects.

▲ Formerly developmental type TA5940.

CD4044AD,CD4044AE,CD4044AK



COS/MOS Quad 3-State R/S Latches

Quad NOR R/S Latch – CD4043A
Quad NAND R/S Latch - CD4044A

Special Features:

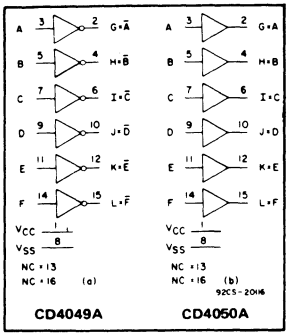
- **Medium Speed Operation**
- **3-Level Outputs with Common Output Enable**
- **Separate Set and Reset Inputs for Each Latch**
- **Low Power TTL Compatible**
- **NOR and NAND Configurations**

Applications:

- **Holding Register in Multi-Register System**
- **Four Bits of Independent Storage with Output Enable**
- **Strobed Register**
- **General Digital Logic**

RCA-CD4043A types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044A types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are gated through transmission gates controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs. The logic operation of the latches is summarized in the truth table below shown in Fig.1.

The CD4043A and CD4044A are supplied in 16-lead dual-in-line ceramic packages (CD4043AD and CD4044AD), 16-lead ceramic flat packs (CD4043AK and CD4044AK), and 16-lead dual-in-line plastic packages (CD4043AE, CD4044AE).



CD4049A CD4050A

COS/MOS Hex Buffer/Converters

CD4049AD, CD4049AE, CD4049AF, CD4049AK — INVERTING TYPE

CD4050AD, CD4050AE, CD4050AF, CD4050AK — NON-INVERTING TYPE

Features:

- Direct Drive to 2 TTL Loads at 5 V, V_{CC} = 5 V, $V_{OL} \leq$ 0.4 V, $I_DN \geq$ 3 mA
- High Source and Sink Current Capability
- General COS/MOS Characteristics

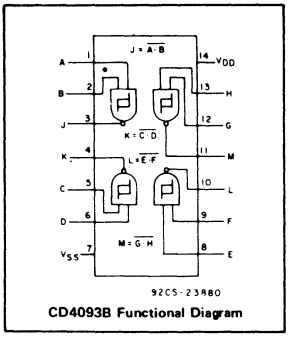
Applications:

- COS/MOS to DTL/TTL Hex Converter
- COS/MOS Current "Sink" or "Source" Driver
- COS/MOS High-to-Low Logic-Level Converter

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC} = 5 V, $V_{OL} \leq$ 0.4 V, and $I_DN \geq$ 3 mA.)

TABLE I

FUNCTION	COS/MOS VOLTAGE RANGE (INPUT)	DTL/TTL VOLTAGE RANGE (OUTPUT)	POWER SUPPLY VOLTAGE RANGE (V_{CC})
HEX LEVEL SHIFTER	3–15 V	3–6 V	3–6 V
HEX INVERTER HEX BUFFER	3–15 V	3–15 V	3–15 V



CD4093B Functional Diagram

COS/MOS Quad 2-Input NAND Schmitt Triggers

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.6 V at V_{DD} = 5 V and 2 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall times
- Standard B-series output drive

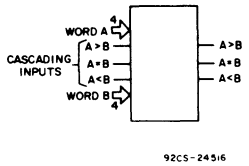
The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

The CD4093B is supplied in 14-lead dual-in-line plastic packages (E), welded-seal ceramic packages (D), ceramic packages (F), ceramic flat packs (K), and in chip form (H).

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



CD4063B Functional Diagram

COS/MOS 4-Bit Magnitude Comparator

Features:

- **Standard B-series output drive**
- **Expansion to 8, 16 . . . 4N bits by cascading units**
- **Medium-speed operation: compares two 4-bit words in 250 ns (typ.) at 10 V**

Applications:

- **Servo motor controls**
- **Process controllers**

The RCA-CD4063B is a low-power 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs ($A < B$, $A = B$, $A > B$) and three cascading inputs ($A < B$, $A = B$, $A > B$) that permit systems designers to expand the comparator function to 8, 12, 16 . . .4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: ($A < B$) = low, ($A = B$) = high, ($A > B$) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs ($A < B$, $A = B$, and $A > B$) on the least significant comparator are connected to a low, a high, and a low level, respectively.

All outputs have equal source- and sink-current capabilities and conform to standard B-series output drive (see Static Electrical Characteristics).

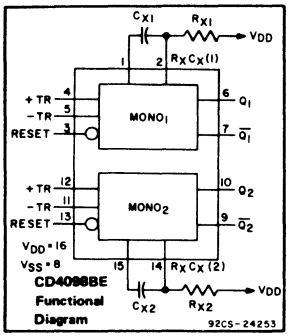
The CD4063B is supplied in 16-lead dual-in-line welded-seal ceramic packages (D), plastic packages (E), ceramic packages (F), flat packs (K), and in chip form (H).

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	X	0	0	1
A3=B3	A2>B2	X	X	X	X	X	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care 1 ≡ High State 0 ≡ Low State

Preliminary CD4098BE



COS/MOS Dual Monostable Multivibrator

Retriggerable/Resettable

Features:

- **Trigger propagation delays independent of R_X, C_X**
- **Triggering from leading or trailing edge**
- **Q and $\overline{Q}$ buffered outputs available**
- **Separate resets**
- **Wide range of output-pulse widths**
- **Equal source and sink currents**

Applications:

- **Pulse delay and timing**
- **Pulse shaping**
- **Astable Multivibrator**

The RCA CD4098BE dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) is independent of R_X and C_X.

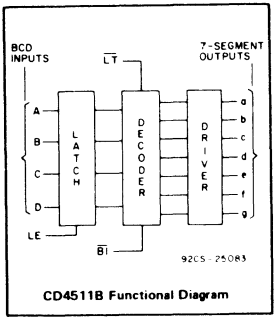
Leading-edge-triggering ($+T_R$) and trailing-edge-triggering ($-T_R$) inputs are provided for triggering from either edge of an input pulse. An unused $+T_R$ input should be tied to V_{SS}. An unused $-T_R$ input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4098BE is not used, its RESET should be tied to V_{SS}. See Table I.

In normal operation, the circuit retriggers on the application of each new pulse. To prevent retriggering when leading-edge triggering is used, $\overline{Q}$ must be connected to $-T_R$. To prevent retriggering when trailing-edge triggering is used, Q must be connected to $+T_R$.

The time period (T) for this multivibrator can be approximated by: $T_X = R_X C_X$. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 1.

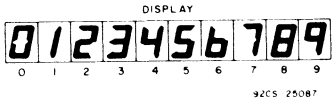
All outputs are independently buffered to provide equal source- and sink-current capabilities. The CD4098BE is available in a 16-lead dual-in-line plastic package (CD4098BE). This device is similar to type MC14528.

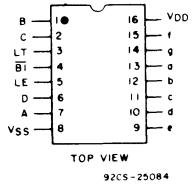
Preliminary CD4511BE



CD4511B Functional Diagram

COS/MOS BCD-to-Seven-Segment Latch Decoder Driver





CD4511B
TERMINAL ASSIGNMENT

The RCA-CD4511B is a BCD-to-Seven-Segment Latch Decoder Driver constructed with COS/MOS logic and n-p-n bipolar transistor output drivers on a single monolithic structure. This device combines the low quiescent power dissipation and high noise immunity features of RCA COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B to drive LED's and other displays directly.

Lamp Test ($\overline{LT}$) Blanking ($\overline{BI}$) and Latch Enable (LE) inputs are provided to test the display, shut off or intensity modulate it, and store a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B is supplied in a 16-lead dual-in-line plastic package (CD4511BE).

This device is similar to type MC14511.

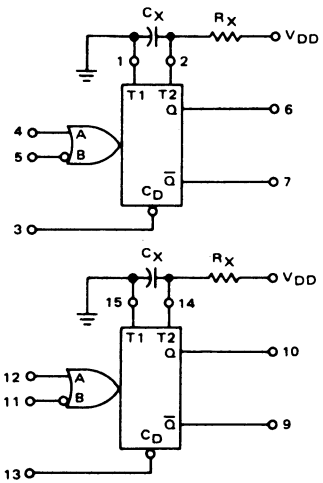
MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

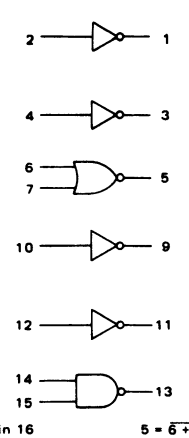
MC14572

HEX GATE

The MC14572 hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Input Impedance = 10^{12} ohms typical
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

$5 = \overline{6 + 7}$
$13 = \overline{14 \cdot 15}$

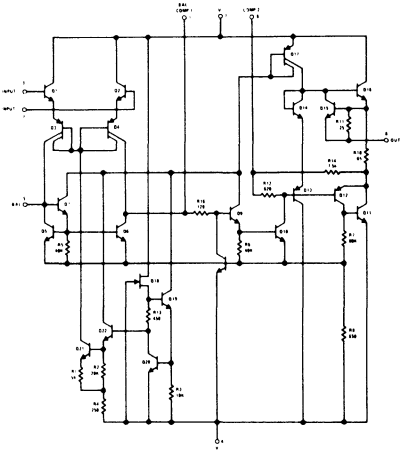
LM301A operational amplifier general description

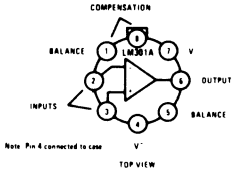
The LM301A is a general-purpose operational amplifier which features improved performance over the 709C and other popular amplifiers. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current.

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the compensation can be tailored to the particular application. For example, as a summing amplifier, slew rates of 10 V/μs and bandwidths of 10 MHz can be realized. In addition, the circuit can be used as a comparator with differential inputs up to ±30V; and the output can be clamped at any desired level to make it compatible with logic circuits.

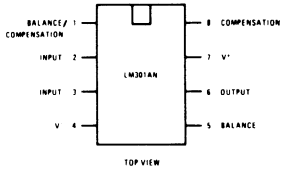
The LM301A provides better accuracy and lower noise than its predecessors in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at reduced cost.

schematic** and connection diagrams





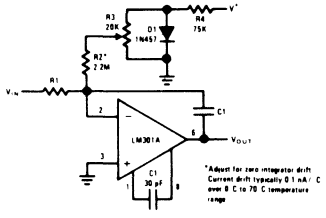
Order Number LM301AH
See Package 11



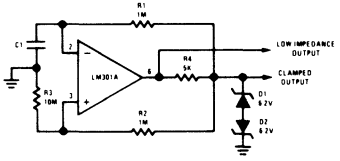
Order Number LM301AN
See Package 20

typical applications **

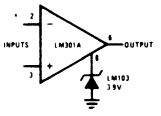
Integrator with Bias Current Compensation



Low Frequency Square Wave Generator



Voltage Comparator for Driving DTL or TTL Integrated Circuits



**Pin connections shown are for metal can.

LM300 voltage regulator

general description

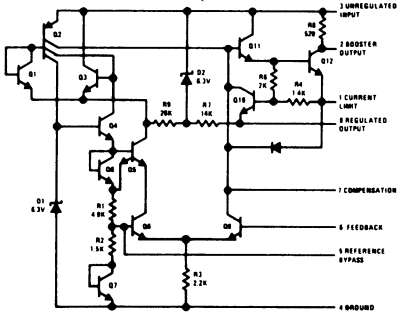
The LM100, LM200 and LM300 are integrated voltage regulators designed for a wide range of applications from digital power supplies to precision regulators for analog circuitry. Built on a single silicon chip, these devices are encapsulated in either an 8-lead, low profile TO-5 header or a 1/4 x 1/4 metal flat package. Outstanding characteristics are:

- Output voltage adjustable from 2V to 30V (LM300 adjustable from 2V to 20V)
- Better than one percent load and line regulation
- One percent temperature stability
- Adjustable short-circuit limiting
- Output currents in excess of 5A possible by adding external transistors
- Can be used as either a linear or high-efficiency switching regulator.

Additional features are fast response to both load and line transients, small standby power dissipation, freedom from oscillations with varying resistive and reactive loads, and the ability to start reliably on any load within rating.

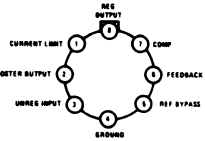
The LM100 is specified for operation over the −55°C to +125°C military temperature range. The LM200 and LM300 are low cost, commercial-industrial versions of the LM100. They are identical to the LM100 except that they are specified for operation from −25°C to 85°C and from 0°C to 70°C respectively.

schematic and connection diagrams



Pin connections shown are for TO-5 package

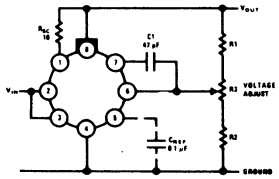
Metal Can Package



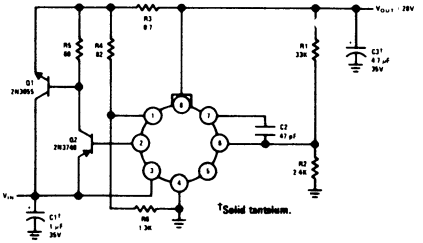
Note: Pin 4 connected to case.
TOP VIEW

typical applications

Basic Regulator Circuit

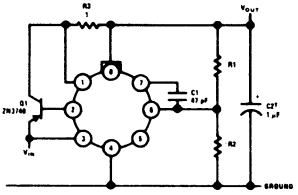


2A Regulator With Foldback Current Limiting



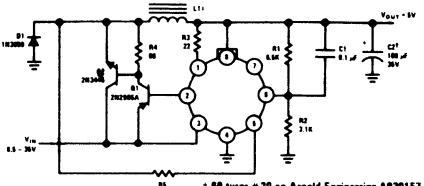
†Solid tantalum.

200 mA Regulator



†Solid tantalum.

4A Switching Regulator



‡ 80 turns # 20 on Arnold Engineering A830157-2 molybdenum permalloy core.

† Solid tantalum.

LM302 voltage follower

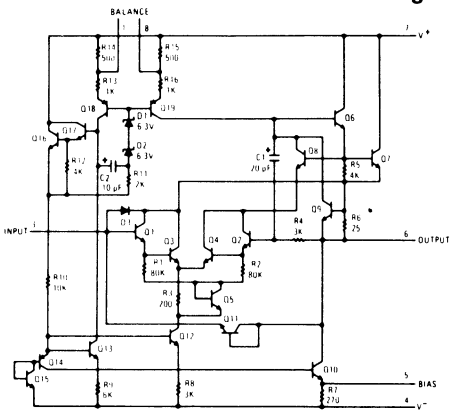
general description

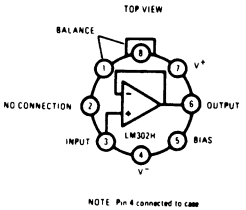
The LM302, an epoxy encapsulated version of the LM102, is a high gain operational amplifier designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the device incorporates advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift. Other outstanding characteristics of the device include:

- Fast Slewing – 10V/μs
- Low input current – 30 nA (max)
- High input resistance – 1,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1K potentiometer
- Specified for operation from 0°C to 70°C
- Plug-in replacement for both the LM201 and LM709C in voltage follower applications.

The LM302, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response – all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

schematic and connection diagrams



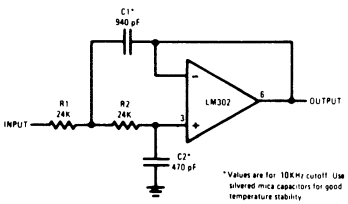


NOTE: Pin 4 connected to case

Order Number LM302H
See Package 11

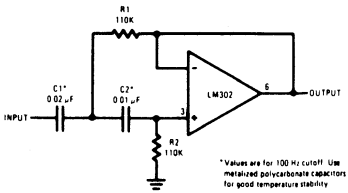
typical applications

Low Pass Active Filter



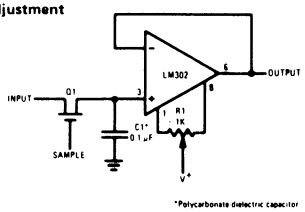
*Values are for 10KHz cutoff. Use silvered mica capacitors for good temperature stability

High Pass Active Filter



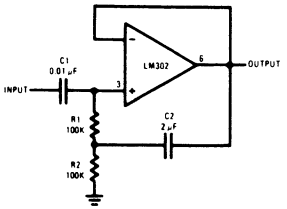
*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability

Sample and Hold With Offset Adjustment



*Polycarbonate dielectric capacitor

High Input Impedance AC Amplifier



LM120 series three-terminal negative regulators

general description

The LM120 Series are three-terminal negative regulators with a fixed output voltage of −5V, −5.2V, −12V, and −15V and up to 1.5A load current capability. These devices need only one external component – a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 Series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

Although primarily intended for fixed output voltage applications, the LM120 Series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation.

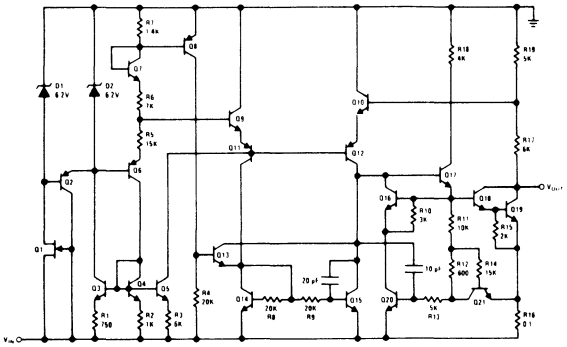
The LM120 Series is available in TO-5 and TO-3 packages. The TO-5 is rated at 200 mA and 2W; the TO-3 at 1A and 20W.

features

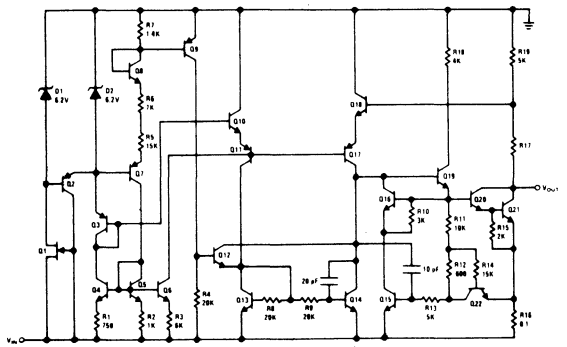
- Preset output voltage error less than ±3%
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- 50 mV load regulation

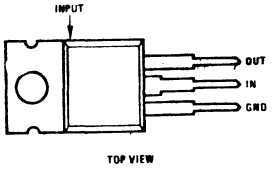
schematic and connection diagrams

−5V & −5.2V



−12V & −15V





TOP VIEW

LM309 five-volt regulator general description

The LM309 is a complete 5V regulator fabricated on a single silicon chip. It is designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The device is available in two common transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulator is essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

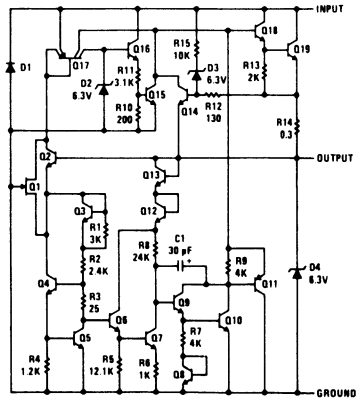
Considerable effort was expended to make the LM309 easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM309 can be set to voltages above 5V, as shown below. It is also possible to use the circuit as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

To summarize, outstanding features of the regulator are:

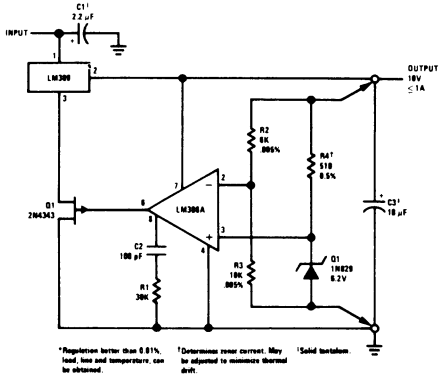
- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

schematic diagram



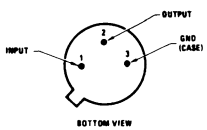
typical application

High Stability Regulator*



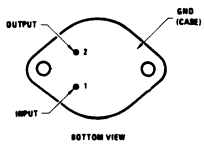
connection diagrams

TO-5 (H)



Order Number LM309H
See Package 9

TO-3 (K)



Order Number LM309K
See Package 18

LM324 quad op amps

general description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard $+5V_{DC}$ power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15\ V_{DC}$ power supplies.

unique characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

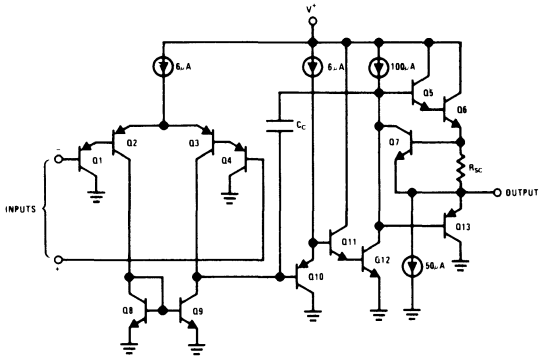
advantages

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

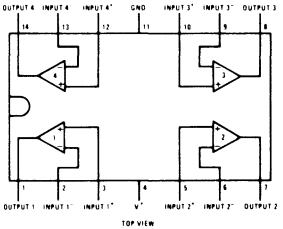
features

- Internally frequency compensated for unity gain
- Large DC voltage gain — 100 dB
- Wide bandwidth (unity gain) (temperature compensated) — 1 MHz
- Wide power supply range:
  Single supply — $3V_{DC}$ to $30V_{DC}$
  or dual supplies — $\pm 1.5V_{DC}$ to $\pm 15V_{DC}$
- Very low supply current drain (800μA) — essentially independent of supply voltage (1 mW/op amp at $+5V_{DC}$)
- Low input biasing current (temperature compensated) — 45 nA_{DC}
- Low input offset voltage — 2 mV_{DC}
  and offset current — 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — $0V_{DC}$ to $V^+ - 1.5V_{DC}$

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number LM124D, LM224D, LM324D, or LM324N
See Package 1 or 22

LM139/LM239/LM339 quad comparators

general description

The LM139 series consists of four independent voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM339 will directly interface with MOS logic – where the low power drain of the LM339 is a distinct advantage over standard comparators.

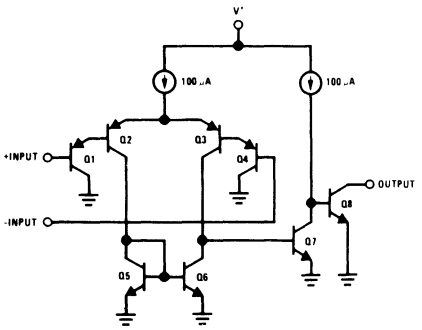
advantages

- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

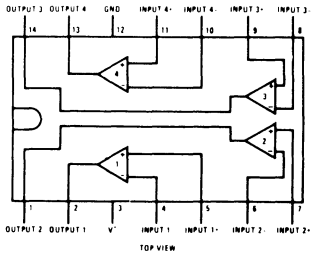
features

- Wide single supply
  Voltage range $2\ V_{DC}$ to $36\ V_{DC}$
  or dual supplies $\pm1\ V_{DC}$ to $\pm18\ V_{DC}$
- Very low supply current drain (0.8 mA) – independent of supply voltage (1 mW/comparator at $+5\ V_{DC}$)
- Low input biasing current 35 nA
- Low input offset current 3 nA
  and offset voltage 3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5μA
  saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL (fanout of 3), DTL, ECL, MOS and CMOS logic systems

schematic and connection diagrams

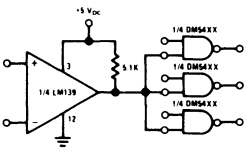


Dual-In-Line and Flat Package

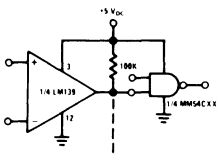


Order Number LM139F	Order Number LM139D, LM239D, or LM339D	Order Number LM339N
See Package 4	See Package 1	See Package 22

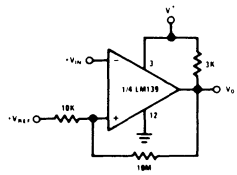
typical applications ($V^+ = 5\ V_{DC}$)



Driving TTL



Driving CMOS



Comparator with Hysteresis

LM340 series 3-terminal positive regulators

general description

The LM340-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

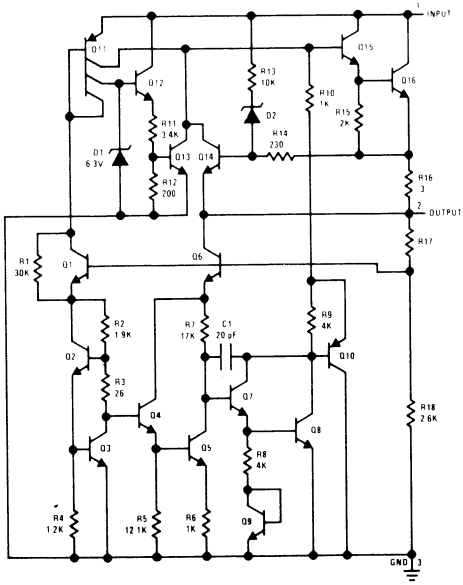
The LM340-XX series is available in two power packages. Both the plastic TO-220 and metal TO-3 packages allow these regulators to deliver over 1.0A if adequate heat sinking is provided. Even with over 1.0A of output current available the regulators are essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM340-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

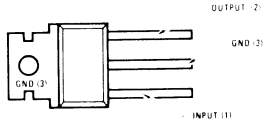
features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-220 and metal TO-3 packages

schematic and connection diagrams



TO-220 (T)



TOP VIEW

LM170/LM270/LM370 agc/squelch amplifier

general description

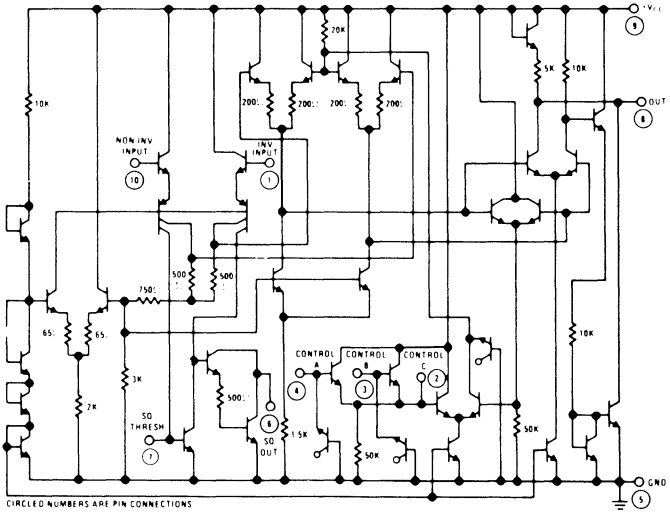
The LM170 is a direct coupled monolithic amplifier whose voltage gain is controlled by an external DC voltage. The device features:

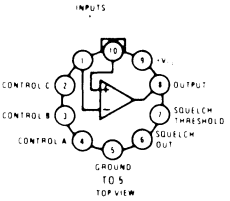
- Large Gain Control Range
- Self-contained AGC/Squelch system, with fast-attack, slow-release.
- Low Distortion
- Minimum DC output shift as gain is varied
- Differential inputs, with large common-mode input range
- Outputs of several amplifiers may be directly summed in multichannel systems.
- Dissipates only 18 mW from +4.5V supply, usable with supply up to +24V.
- Sensitive squelch threshold set by single external resistor.

In addition to communication system squelch and AGC applications, the LM170 is useful as constant-amplitude audio oscillator, linear low frequency modulator, single-sideband automatic load control, and as a variable DC gain element in analog computation.

The LM170 is specified for operation over the -55 C to +125 C military temperature range. The LM270 is specified for operation over the -25 C to +75 C temperature range. The LM370 is specified for operation over the 0 C to +70 C temperature range.

schematic** and connection diagrams

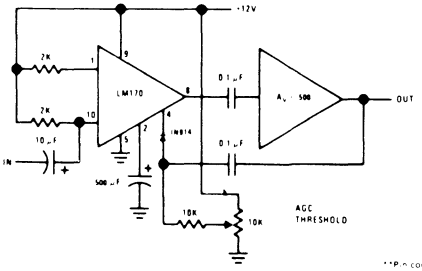




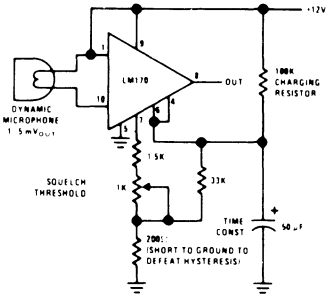
Order Number LM170H or LM270H or LM370H
See Package 14

typical applications**

AGC Using Built-in Detection, Driven By Additional System Gain



Squelched Preamplifier with Hysteresis



**Pin connections shown are for metal can

LM171/LM271/LM371 integrated rf/if amplifier

general description

The LM171/LM271/LM371 is a monolithic RF-IF amplifier capable of emitter coupled or cascode operation from DC to 250 MHz. Wide versatility is offered by having all inputs and outputs brought out so many circuit configurations are possible.

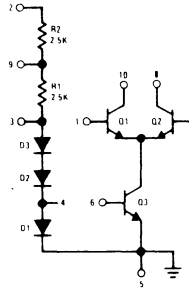
features

- Low internal feedback, allowing high stability-limited gain
- Versatility through user-connected configurations
- As emitter coupled amplifier, symmetrical, non-saturated limiting
- As cascode, wide AGC range with constant input admittance
- As differential DC amplifier, low input offset voltage and wide dynamic range
- As video amplifier, externally selected gain, and high gain-bandwidth product
- 100 MHz tuned power gain

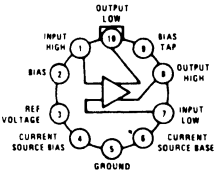
(Emitter Coupled)	24.6 dB
(Cascode)	27.5 dB

In addition to amplifier service, the circuit is useful in mixer, oscillator, detector, modulator, and numerous other applications. The LM271 is a plug-in replacement for the 911C type.

schematic and connection diagrams



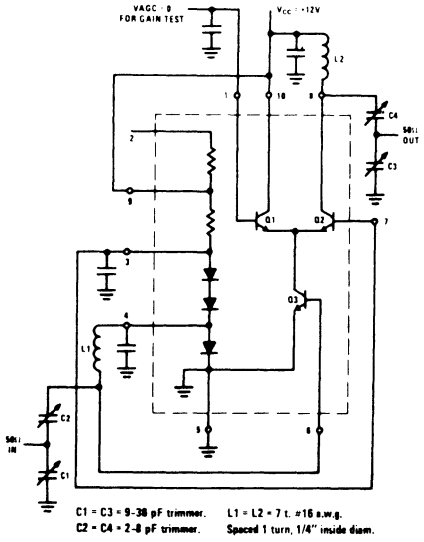
Metal Can Package



Order Number LM171H
or LM271H or LM371H
See Package 14

typical applications

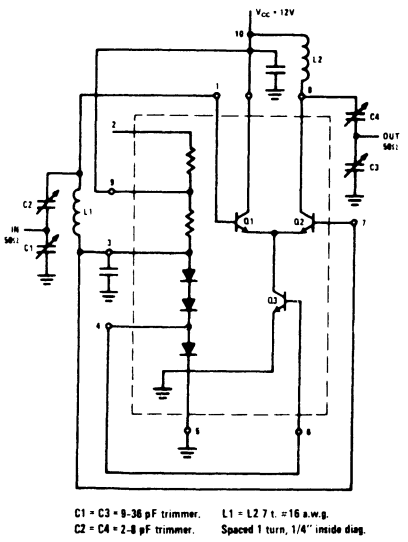
100 MHz Cascode Test Circuit



C1 = C3 = 9-36 pF trimmer. L1 = L2 = 7 t. #16 a.w.g.
C2 = C4 = 2-8 pF trimmer. Spaced 1 turn, 1/4" inside diam.

FIGURE 1

100 MHz Emitter Coupled Test Circuit



C1 = C3 = 9-36 pF trimmer. L1 = L2 7 t. #16 a.w.g.
C2 = C4 = 2-8 pF trimmer. Spaced 1 turn, 1/4" inside diag.

FIGURE 2

Note: All unmarked bypass capacitors 1000 pF.

LM274/LM374 am/fm/ssb if video amp/detector

general description

The LM273/LM373 and LM274/LM374 are broadband communications subsystems, capable of performing the diverse functions required in AM, FM or single sideband receivers and transmitters. In addition, the LM274/LM374 may operate as high gain AGC'd video amplifier. Bandpass shaping may be performed by a single external filter, connected between amplifier sections, at frequencies from audio up to 30 MHz. The first section of the LM273/LM373 is optimized to drive low impedance loads, such as mechanical or ceramic filters. The LM274/LM374 has a high output impedance, ideal for high-Z crystal, LC or ceramic filters.

The LM273 and LM274 are specified for operation over the −25°C to +100°C military temperature range. The LM373 and LM374 are specified for operation over the 0°C to +70°C temperature range.

features

CONNECTED FOR AM OPERATION

- High gain; typical sensitivity of 10 μV at 455 kHz
- Wide bandwidth; 30 MHz capability
- Self-contained detector and AGC system
- Wide AGC range, greater than 60 dB for a 10 dB output change at 27 MHz
- Less than ±1 dB change in audio output −20°C to +100°C, typically
- Access to detector input for S/N improvement
- No DC paths required through external filters
- Low feedthrough between amplifier sections, typically better than 65 dB

CONNECTED FOR FM OPERATION

- Three emitter coupled limiting stages and simple quadrature detector
- Detection of ±5 kHz deviation FM at either 455 kHz or 10.7 MHz
- Two separated amplifier blocks, allowing filtering in two or more blocks
- No DC paths required through external filters or through quadrature network

CONNECTED FOR SSB OPERATION

- Double balanced product detector
- Self contained audio peak AGC system
- Easy external tailoring of AGC characteristic for desired AGC figure of merit

CONNECTED FOR VIDEO AMPLIFIER OPERATION

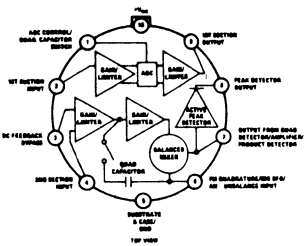
- Internal video peak detector for video AGC
- High and low level video outputs
- Gated video AGC capability

In addition, these versatile microcircuits may be used as:

- Constant amplitude or amplitude modulated RF oscillator
- Synchronous demodulating IF strip
- Mixer and IF, using AGC section as a mixer
- Double sideband modulator with audio AGC

connection diagrams

Metal Can Package



Order Number LM273H or LM373H
LM274H or LM374H
See Package 14

LM380 audio power amplifier

general description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self entering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout. A mini dual-in-line package version with reduced power capability also available.

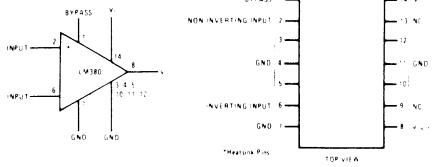
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters,etc.

features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

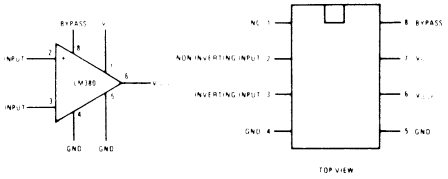
block and connection diagrams

Dual-In-Line Package



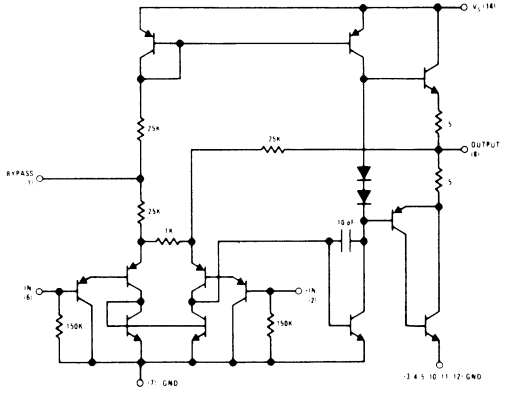
Order Number LM380N
See Package 22

Dual-In-Line Package



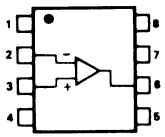
Order Number LM380N-8
See Package 20

schematic diagram



531

The 531 is a fast slewing high performance operational amplifier which retains D.C. performance equal to the best general purpose types while providing far superior large signal A.C. performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier can be compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

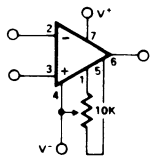


1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NO. NE531V

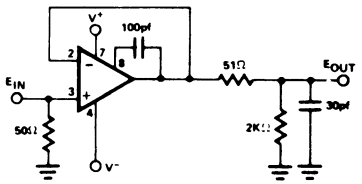
- **35V/μsec SLEW RATE AT UNITY GAIN**
- **PIN FOR PIN REPLACEMENT FOR μA709, μA748 OR LM101**
- **COMPENSATED WITH A SINGLE CAPACITOR**
- **SAME LOW DRIFT OFFSET NULL CIRCUITRY AS μA741**
- **SMALL SIGNAL BANDWIDTH 1 MHz**
- **LARGE SIGNAL BANDWIDTH 500KHz**
- **TRUE OP AMP D.C. CHARACTERISTICS MAKE THE 531 THE IDEAL ANSWER TO ALL SLEW RATE LIMITED OPERATIONAL AMPLIFIER APPLICATIONS.**

OFFSET NULL CIRCUIT



Supply Voltage	±22V
Internal Power Dissipation	300mW
Differential Input Voltage	±15V
Common Mode Input Voltage	±15V
Voltage Between Offset Null and V^-	±0.5V
Operating Temperature Range	
NE531	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

TRANSIENT RESPONSE TEST CIRCUIT



540

DESCRIPTION

The 540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

FEATURES

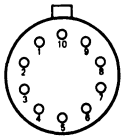
- **INTERNAL CURRENT LIMITING**
- **LOW STANDBY CURRENT**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **WIDE POWER BANDWIDTH**
- **LOW DISTORTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 27 Volts SE540
	± 22 Volts NE540
Operating Temperature Range	-55°C to +125°C SE540
	0°C to +70°C NE540
Storage Temperature Range	-65°C to +150°C
Output Short Circuit Duration (Not exceeding maximum dissipation.)	Indefinite

PIN CONFIGURATION (TOP VIEW)

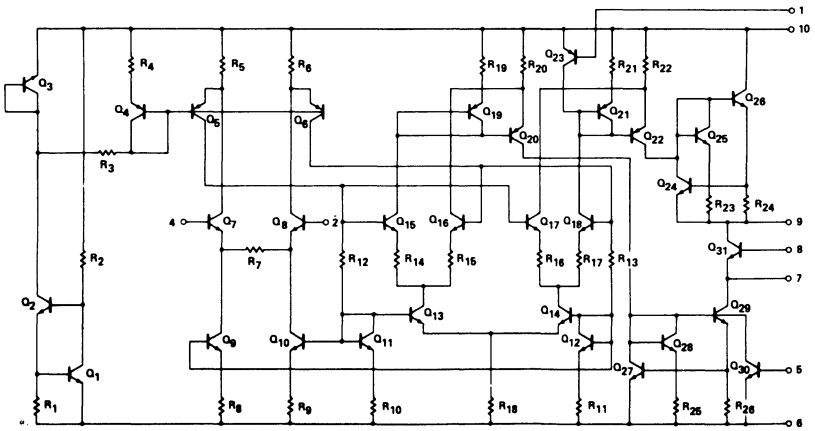
L PACKAGE



1. Power Limit
2. Non Inverting Input
3. NC
4. Inverting Input
5. Power Limit
6. V^-
7. Output 1 (emmitter)
8. Output 2 (base)
9. Output 3 (collector)
10. V^+

ORDER PART NOS. SE540L/NE540L

SCHEMATIC



LM555/LM555C timer

general description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

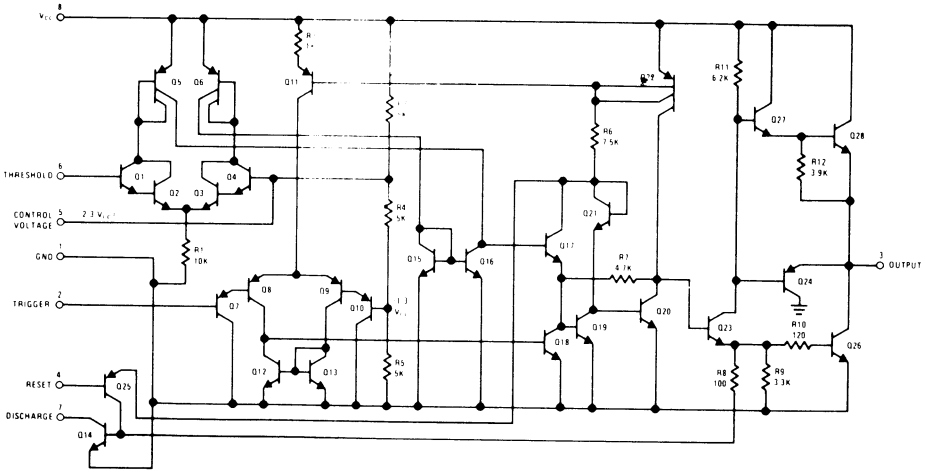
features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200mA
- Output and supply TTL compatible
- Temperature stability better than .005% per C
- Normally on and normally off output

applications

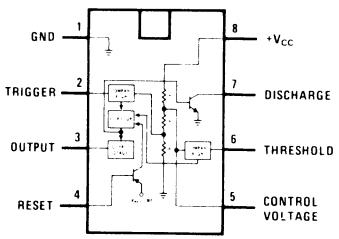
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

schematic diagram



connection diagrams

Dual-In-Line Package



TOP VIEW

Order Number LM555CN

See Package 20

LM556/LM556C dual timer

general description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

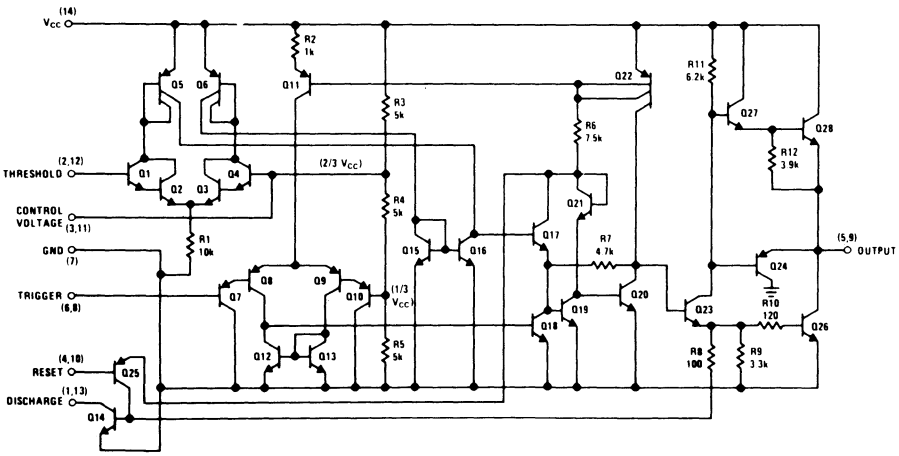
features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

applications

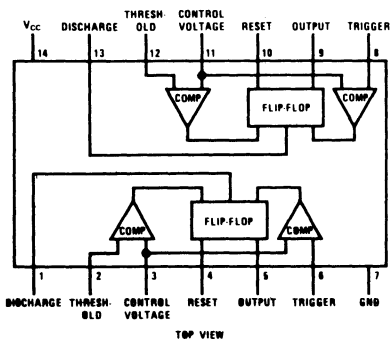
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

schematic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number LM556D or LM556CD
See Package 1
Order Number LM556CN
See Package 22
Order Number LM556J or LM556CJ
See Package 16

LM565/LM565C phase locked loop

general description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CH and LM565CN are specified for operation over the 0°C to +70°C temperature range.

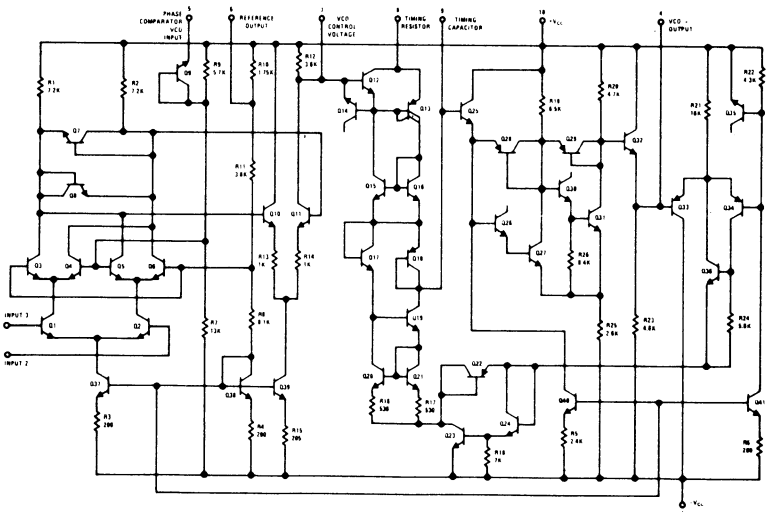
features

- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%.

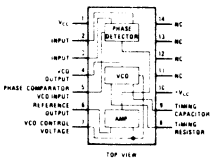
applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators.

schematic and connection diagrams



Dual-In-Line Package



Order Number LM565CN
See Package 22

LM566/LM566C voltage controlled oscillator

general description

The LM566/LM566C are general purpose voltage controlled oscillators which may be used to generate square and triangular waves, the frequency of which is a very linear function of a control voltage. The frequency is also a function of an external resistor and capacitor.

The LM566 is specified for operation over the −55°C to +125°C military temperature range. The LM566C is specified for operation over the 0°C to +70°C temperature range.

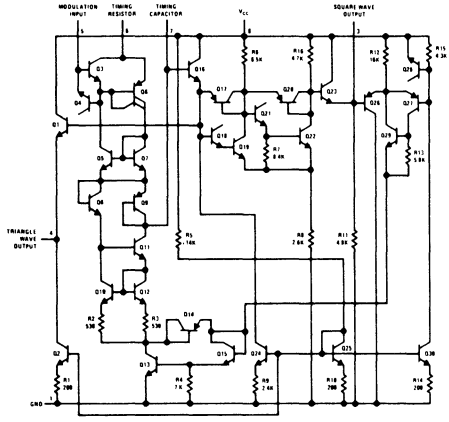
features

- Wide supply voltage range: 10 to 24 volts
- Very linear modulation characteristics
- High temperature stability
- Excellent supply voltage rejection
- 10 to 1 frequency range with fixed capacitor
- Frequency programmable by means of current, voltage, resistor or capacitor.

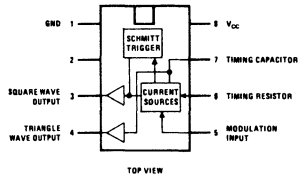
applications

- FM modulation
- Signal generation
- Function generation
- Frequency shift keying
- Tone generation

schematic and connection diagrams



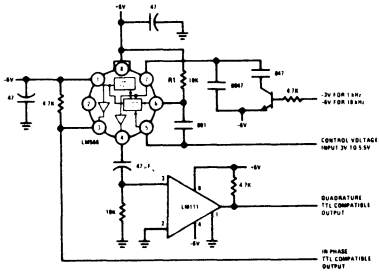
Dual-In-Line Package



Order Number LM566CN
See Package 20

typical application

1 kHz and 10 kHz TTL Compatible Voltage Controlled Oscillator



applications information

The LM566 may be operated from either a single supply as shown in this test circuit, or from a split (±) power supply. When operating from a split supply, the square wave output (pin 4) is TTL compatible (2 mA current sink) with the addition of a 4.7 kΩ resistor from pin 3 to ground.

A .001 μF capacitor is connected between pins 5 and 6 to prevent parasitic oscillations that may occur during VCO switching.

$$f_O = \frac{2(V^+ - V_5)}{R_1 C_1 V^+}$$

where

$2K < R_1 < 20K$

and V_5 is voltage between pin 5 and ground.

LM567/LM567C tone decoder

general description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

features

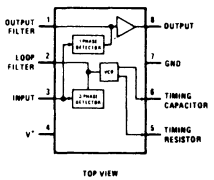
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

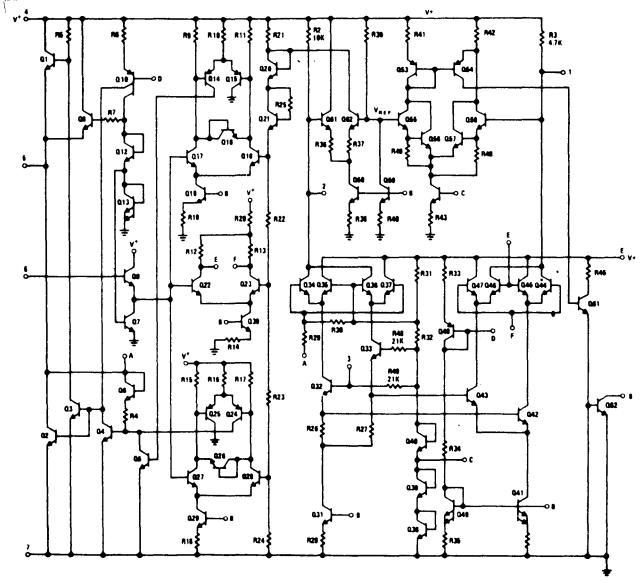
schematic and connection diagrams

Dual-In-Line Package



TOP VIEW

Order Number LM567CN
See Package 20



LM703L low power drain rf/if amplifier

general description

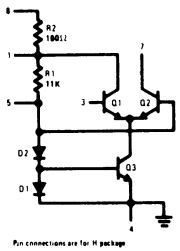
The LM703L is a monolithic RF-IF amplifier, having an efficient DC biasing system, reducing demands upon power supply and decoupling elements. Its low internal feedback guarantees a high stability-limited gain.

Applications include limiting and nonlimiting amplifiers, mixers, and RF oscillators. The LM703L is specifically characterized for operation in consumer applications such as TV sound IF, FM-IF limiter amplifier, and Chroma reference oscillator for color TV.

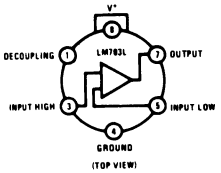
features

- Power Consumption 96 mW (max.)
- Forward Transadmittance 33 mmhos
- Input Conductance 0.35 mmhos
- Output Conductance 0.03 mmhos
- Peak-to-Peak Output Current 5.0 mA

schematic and connection diagrams



Pin connections are for H package

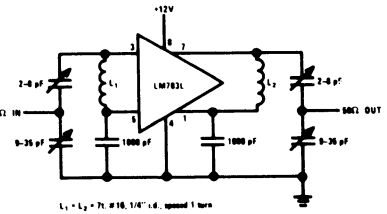


NOTE Pin 4 connected to case

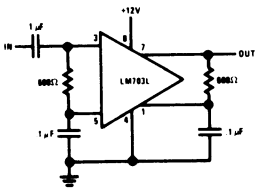
Order Number LM703LH
See Package 10

typical applications

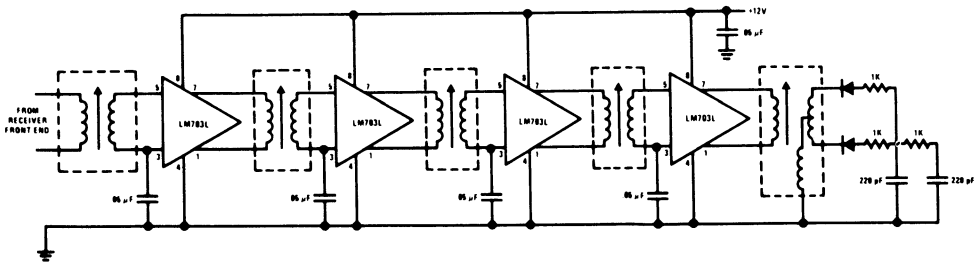
100 MHz Narrow Band Amplifier



RC Coupled Video Amplifier



Four Stage 10.7 MHz FM-IF Amplifier



LM709 operational amplifier

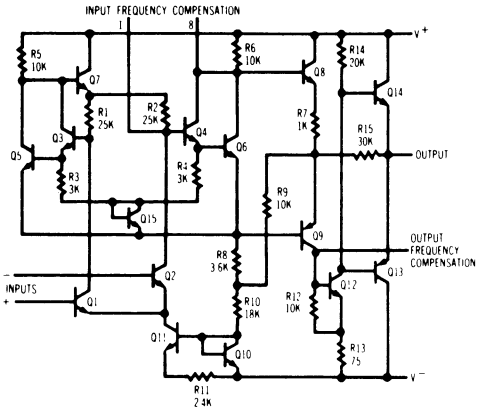
general description

The LM709 is a monolithic operational amplifier intended for general-purpose applications. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. Further, the class-B output stage gives a large output capability with minimum power drain.

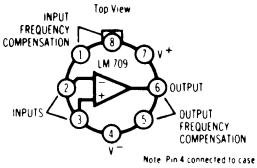
External components are used to frequency compensate the amplifier. Although the unity-gain compensation network specified will make the amplifier unconditionally stable in all feedback configurations, compensation can be tailored to optimize high-frequency performance for any gain setting.

The fact that the amplifier is built on a single silicon chip provides low offset and temperature drift at minimum cost. It also ensures negligible drift due to temperature gradients in the vicinity of the amplifier.

schematic and connection diagrams



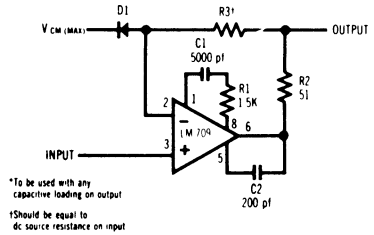
Metal Can



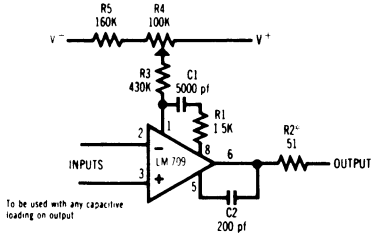
Order Number LM709H
See Package 11

typical applications*

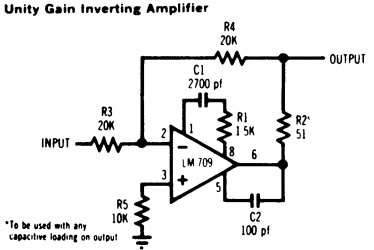
Voltage Follower



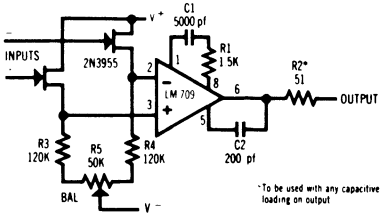
Offset Balancing Circuit



Unity Gain Inverting Amplifier



FET Operational Amplifier



* Pin connections shown are for Metal Can package.

LM710C voltage comparator

general description

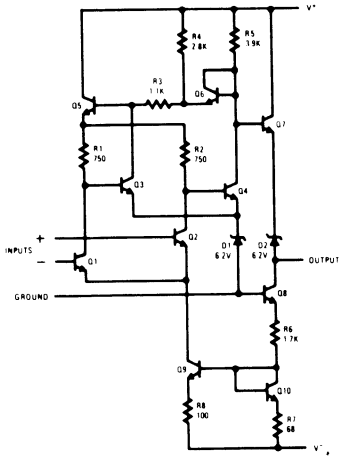
The LM710C is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

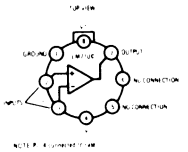
The LM710C is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

The LM710C is the commercial/industrial version of the LM710A. It is identical to the LM710A except that operation is specified over a 0°C to 70°C temperature range.

schematic* and connection diagrams

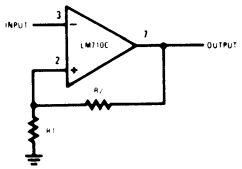


Metal Can Package

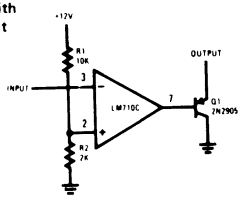


typical applications*

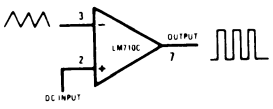
Schmidt Trigger



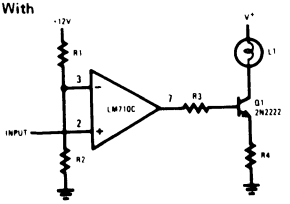
Line Receiver With Increased Output Sink Current



Pulse Width Modulator



Level Detector With Lamp Driver



*Pin connections shown are for metal can.

μA739

DUAL LOW NOISE AUDIO PREAMPLIFIER/OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION – The μA739 consists of two identical monolithic Operational Amplifiers using the Fairchild Planar* epitaxial process. These low noise, high gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

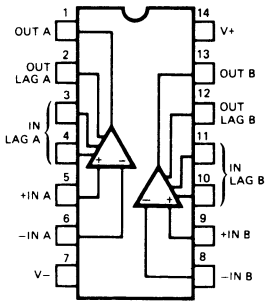
- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	670 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Hermetic	−65°C to +150°C
Molded	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA739C	μA739DC
μA739C	μA739PC

LM741/LM741C operational amplifier

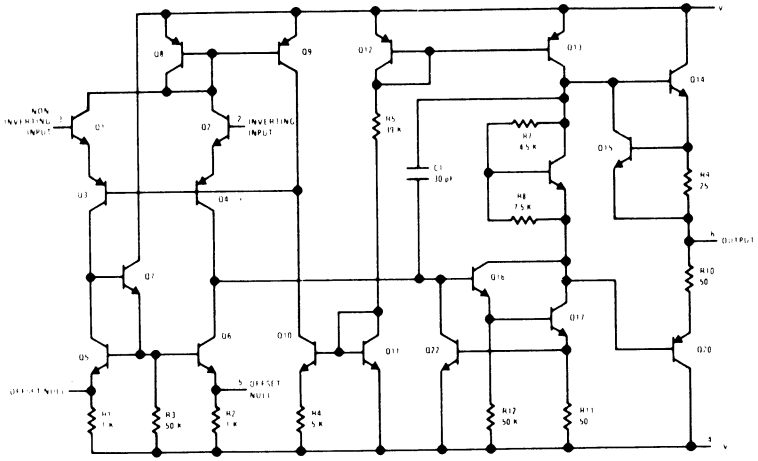
general description

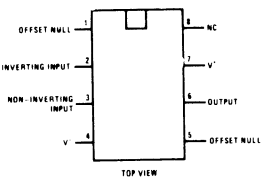
The LM741 and LM741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741 except that the LM741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of -55°C to 125°C.

schematic and connection diagrams





Order Number LM741CN

See Package 20

LM747/LM747C dual operational amplifier

general description

The LM747 and the LM747C are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

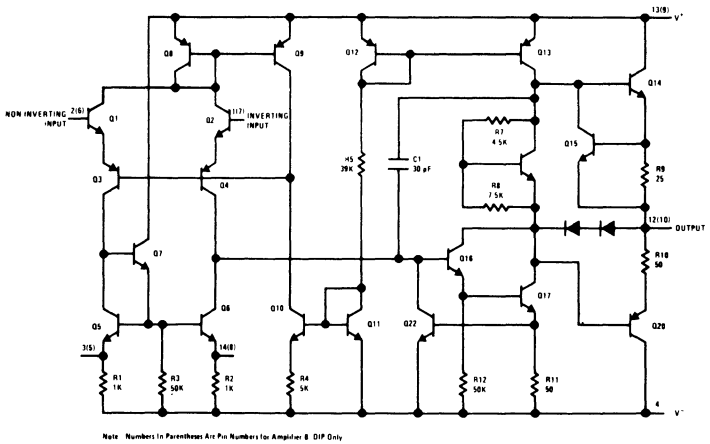
features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- No latch-up
- Balanced offset null

Additional features of the LM747 and LM747C are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

The LM747C is identical to the LM747 except that the LM747C has its specifications guaranteed over the temperature range from 0°C to 70°C instead of −55°C to +125°C.

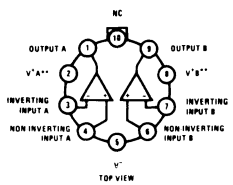
schematic diagram (each amplifier)



Note: Numbers in Parentheses Are Pin Numbers for Amplifier B. DIP Only.

connection diagrams

Metal Can Package



Order Number LM747H or LM747CH
See Package 14

**V+A and V+B are internally connected.

LM748/LM748C operational amplifier

general description

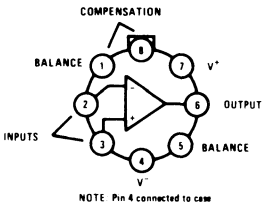
The LM748/LM748C is a general purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients. In addition, the device features:

- Frequency compensation with a single 30 pF capacitor
- Operation from ±5V to ±20V
- Low current drain: 1.8 mA at ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded.
- Same pin configuration as the LM101.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

The LM748 is specified for operation over the −55°C to +125°C military temperature range. The LM748C is specified for operation over the 0°C to +70°C temperature range.

connection diagrams

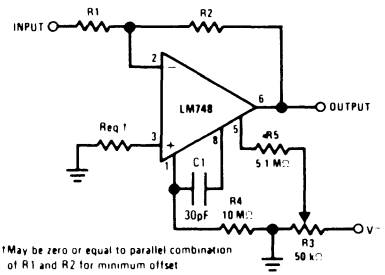


NOTE: Pin 4 connected to case

Order Number LM748H or LM748CH
See Package 11

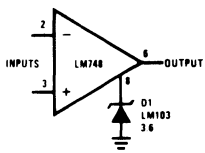
typical applications

Inverting Amplifier with Balancing Circuit

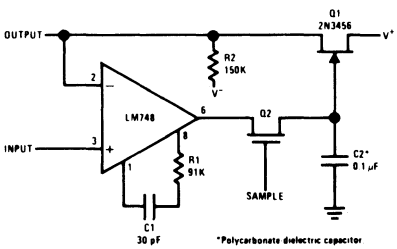


†May be zero or equal to parallel combination of R1 and R2 for minimum offset

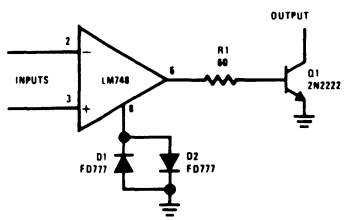
Voltage Comparator for Driving DTL or TTL Integrated Circuits



Low Drift Sample and Hold



Voltage Comparator for Driving RTL Logic or High Current Driver



LM2900 quad amplifier

general description

The LM2900 consists of four independent, dual input, internally compensated amplifiers which were designed specifically for automotive and industrial applications. They operate off a single power supply voltage and provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function.

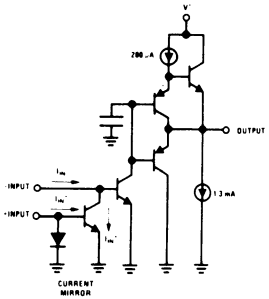
Applications include: AC amplifiers, RC active filters; low frequency triangle, squarewave and pulse waveform generation circuits; tachometers and low speed, high voltage digital logic gates.

For additional information, see Application Note 72, "The LM3900 – A New Current-Differencing Quad of ± Input Amplifiers."

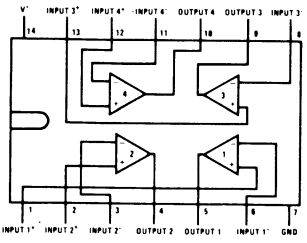
features

- Wide single supply voltage range — 4 V_{DC} to 36 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current — 30 nA
- High open-loop gain — 70 dB
- Wide bandwidth — 2.5 MHz (Unity Gain)
- Larger gain-bandwidth product in non-inverting mode (A_V = 100 @ f = 1 MHz)
- Large output voltage swing — (V^+ −1) V_{PP}
- Internally frequency compensated for unity gain
- Output short-circuit protection
- Eliminates need for dual supplies
- Reduces package count

schematic and connection diagrams

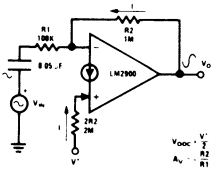


Dual-In-Line Package

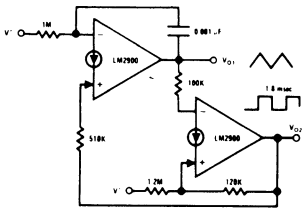


Order Number LM2900N
See Package 22

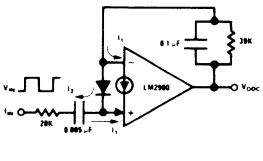
typical applications (V^+ = 15V_{DC})



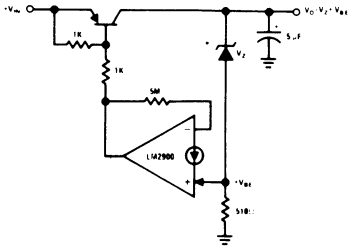
Inverting Amplifier



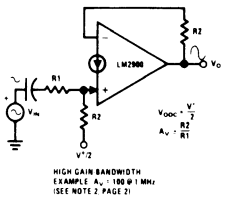
Triangle/Square Generator



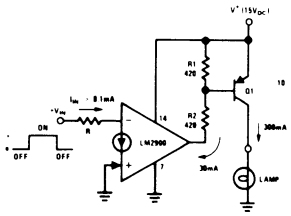
Frequency-Doubling Tachometer



Low V_{IN}–V_{OUT} Voltage Regulator



Non-Inverting Amplifier



Boosting to 300 mA Loads

LM1558/LM1458 dual operational amplifier

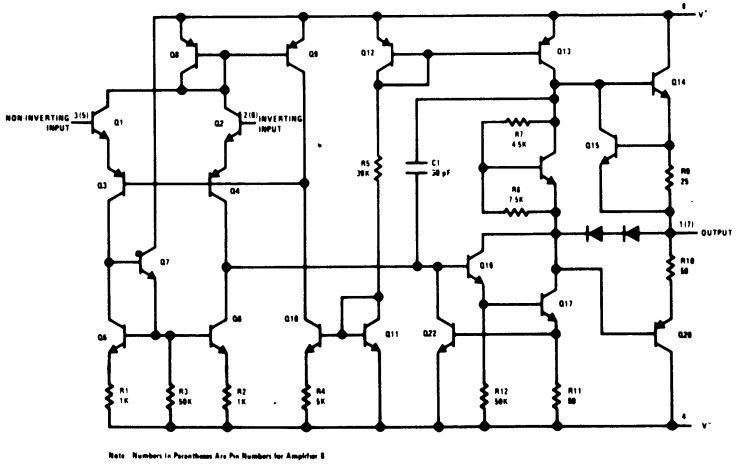
general description

The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

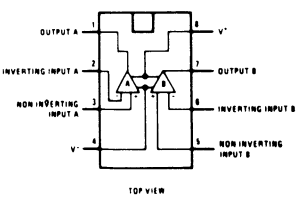
The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to 70°C instead of −55°C to +125°C.

schematic and connection diagrams



Note: Numbers in Parentheses Are Pin Numbers for Amplifier B

Dual-In-Line Package



TOP VIEW

Order Number LM1458N
See Package 20

LM1596/LM1496 balanced modulator-demodulator

general description

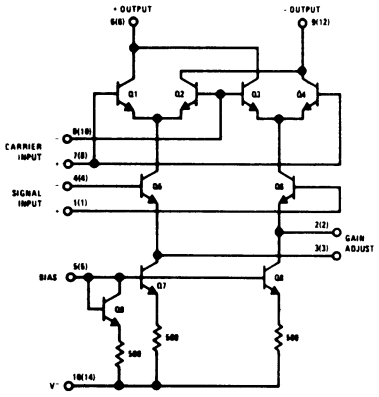
The LM1596/LM1496 are double balanced modulator-demodulators which produce an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection, broadband frequency doubling and chopping.

The LM1596 is specified for operation over the −55°C to +125°C military temperature range. The LM1496 is specified for operation over the 0°C to +70°C temperature range.

features

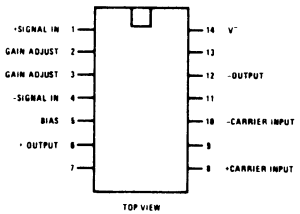
- Excellent carrier suppression
  - 65 dB typical at 0.5 MHz
  - 50 dB typical at 10 MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- Low offset and drift
- Wide frequency response up to 100 MHz

schematic and connection diagrams



Numbers in parentheses show DIP connections.

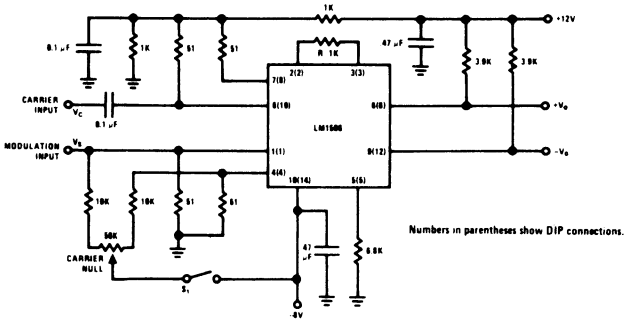
Dual-In-Line Package



TOP VIEW

Order Number LM1496J or LM1596J
See Package 16
Order Number LM1496N
See Package 22

typical application and test circuit



Numbers in parentheses show DIP connections.

Note: S_1 is closed for "adjusted" measurements.

Suppressed Carrier Modulator

PRECISION WAVEFORM GENERATOR/VOLTAGE CONTROLLED OSCILLATOR

8038

FEATURES

- Low Frequency Drift With Temperature – 50ppm/°C Max.
- Simultaneous Outputs – Sine-Wave, Square-Wave and Triangle.
- High Level Outputs – T^2L to 28V
- Low Distortion – 1%
- High Linearity – 0.1%
- Easy to Use – 50% Reduction in External Components.
- Wide Frequency Range of Operation 0.001Hz to 1.0MHz
- Variable Duty Cycle – 2% to 98%

GENERAL DESCRIPTION

The 8038 Waveform Generator is a monolithic integrated circuit, capable of producing sine, square, triangular, sawtooth and pulse waveform of high accuracy with a minimum of external components (refer to Figures 8 and 9) The frequency (or repetition rate) can be selected externally over a range from less than 1/1000Hz to more than 1MHz and is highly stable over a wide temperature and supply voltage range. Frequency modulation and sweeping can be accomplished with an external voltage and the frequency can be programmed digitally through the use of either resistors or capacitors. The Waveform Generator utilizes advanced monolithic technology, such as thin film resistors and Schottky-barrier diodes. The 8038 Voltage Controlled Oscillator can be interfaced with phase lock loop circuitry to reduce temperature drift to below 50ppm/°C.

FUNCTIONAL DIAGRAM

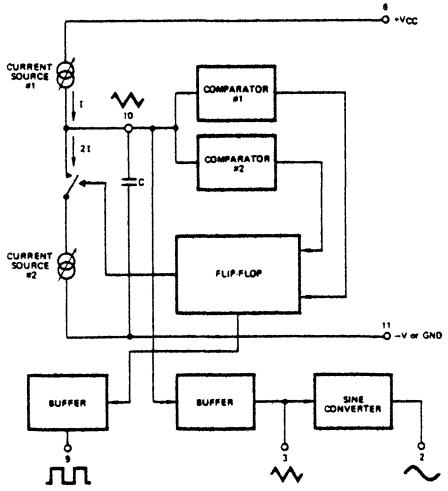
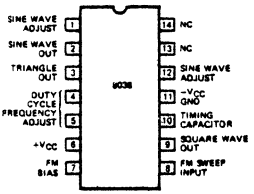


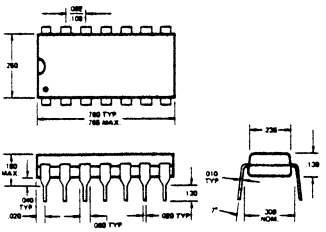
FIGURE 1. BLOCK-DIAGRAM OF WAVEFORM GENERATOR.

CONNECTION DIAGRAM

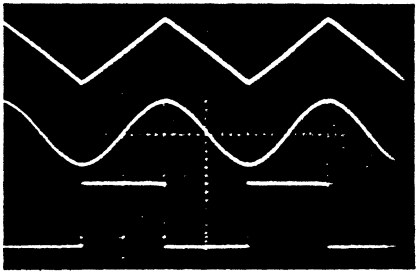


PACKAGE DIMENSIONS

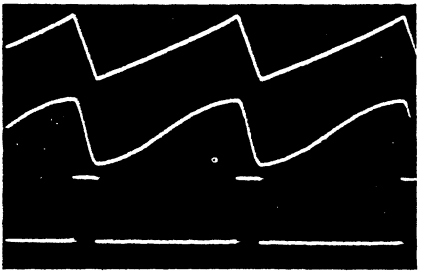
DIP



THEORY OF OPERATION



SQUARE-WAVE DUTY CYCLE – 50%



SQUARE-WAVE DUTY CYCLE – 20%

FIGURE 7. PHASE RELATIONSHIP OF WAVEFORMS.

The performance of the sine-wave output is shown in Figure 5. Figure 6 shows additional general information concerning current consumption and frequency stability and Figure 7 shows the phase relationship between the three waveforms.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 8. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 0 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{CC}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{CC} \times R_A}{1/5 \times V_{CC}} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 1 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V_{CC}}{\frac{2}{5} \times \frac{V_{CC}}{R_B} - \frac{1}{5} \times \frac{V_{CC}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 8b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorter together, as shown in Figure 8c. This connection, however, carries an inherently larger variation of the duty-cycle.

With two separate timing resistors, the *frequency* is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{RC} \qquad \text{(for Figure 8a)}$$

If a single timing resistor is used (Figures 8b and c), the frequency is

$$f = \frac{0.15}{RC}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the

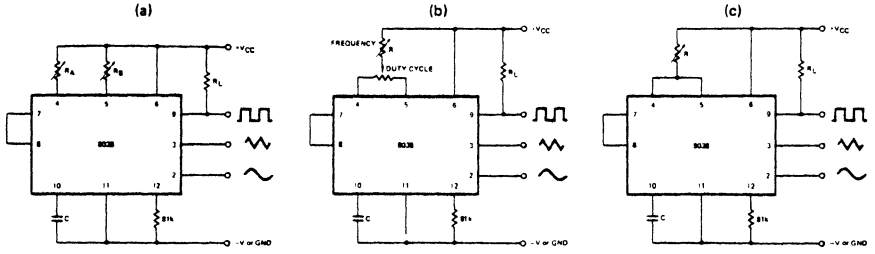


FIGURE 8. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS.

fact that both currents *and* thresholds are direct, linear function of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 81kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 9. This configuration allows a reduction of sine-wave distortion close to 0.5%.

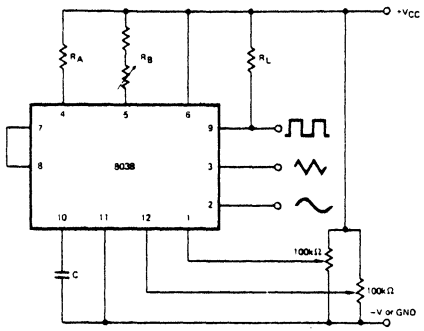


FIGURE 9. CONNECTION TO ACHIEVE MINIMUM SINE-WAVE DISTORTION.

SELECTING R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work. However certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5 mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will be obtained for charging currents of 10μA to 1 mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times V_{CC}}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{V_{CC}}{5R_A}$$

A similar calculation holds for R_B.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between +V and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from $+V_{CC}$). By altering this voltage, frequency modulation is performed.

For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing dc decoupling with a capacitor, as shown in Figure 10a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance. Without it (i.e. terminals 7 and 8 connected together), the input impedance is 8kΩ; with it, this impedance increases to (R+8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 10b). In this way the entire bias for the current sources is created by the modulating signal and a very large (e.g. 1000:1) sweep range is created (f = 0 at V_{sweep} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept from V_{CC} to 2/3 V_{CC}.

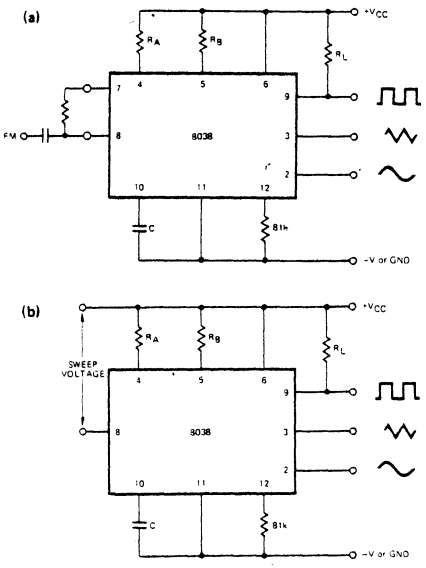


FIGURE 10. CONNECTIONS FOR FREQUENCY MODULATION (a) AND SWEEP (b).

MM5309, MM5311, MM5312, MM5313, MM5314, MM5315 digital clocks

general description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion implanted, depletion mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (4 or 6-digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11V to 19V and do not require a regulated supply. These clocks are packaged in dual-in-line packages.

features

- 50 or 60 Hz operation
- 12 or 24-hour display format
- Leading-zero blanking (12-hour format)
- 7-segment outputs
- Single power supply
- Fast and slow set controls
- Internal multiplex oscillator
- For features of individual clocks, see Table I

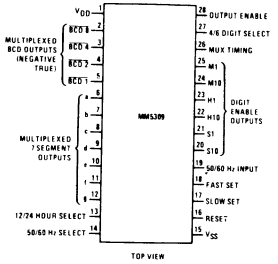
applications

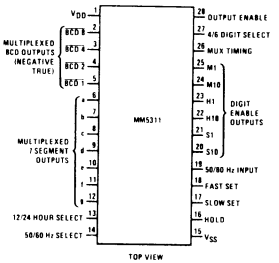
- Desk clocks
- Automobile clocks
- Industrial clocks
- Interval Timers

TABLE I.

FEATURES	MM5309	MM5311	MM5312	MM5313	MM5314	MM5315
$\overline{BCD}$ Outputs	X	X	X	X		X
4/6-Digit Display Mode	X	X		X	X	X
Hold Count Control		X		X	X	X
1 Hz Output			X	X		
Output Enable Control	X	X			X	
Reset	X					X

connection diagrams (Dual-In-Line Packages)





absolute maximum ratings

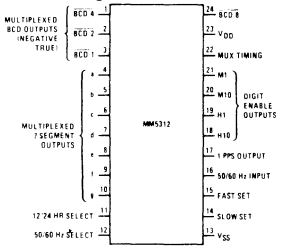
Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} −,20V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

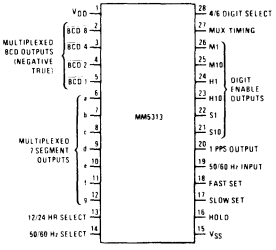
electrical characteristics

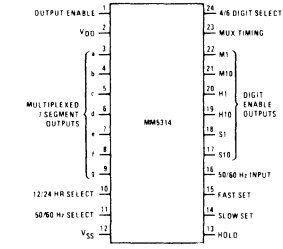
T_A within operating range, V_{SS} = 11V to 19V, V_{DD} = 0V, unless otherwise specified.

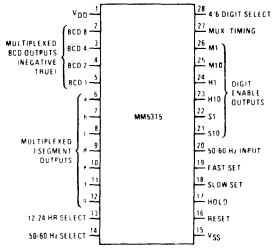
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11		19	V
Power Supply Current	V_{SS} = 14V, (No Output Loads)			10	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−10	V
Multiplex Frequency	Determined by External R & C	0.100	1.0	60	kHz
All Logic Inputs	Driven by External Timebase	dc		60	kHz
Logical High Level	Internal Depletion Device to V_{SS}	V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−10	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2 kΩ to V_{DD}	2.0		20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100 Ω to V_{SS}	5.0		25	mA sink

connection diagrams (Continued) Dual-In-Line Packages (Top Views)









MM5375AA/MM5375AB/MM5375AC/ MM5375AD/MM5375AE digital alarm clock

general description

The MM5375 digital alarm clock is a monolithic MOS integrated circuit utilizing p-channel low threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic to give a four or six digit twelve or twenty-four hour display from a 50 or 60 Hz input. Inputs include time setting, 60 Hz input, display brightness control, alarm set, snooze, alarm off, and multiplex oscillator frequency control. Outputs consist of 8-segment selects (eighth segment for AM/PM and colon indications), digit enables, and alarm signal consisting of a 500 Hz to 1,000 Hz, squarewave (frequency externally adjustable) gated on and off at a 2.0 Hz rate. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication.

features

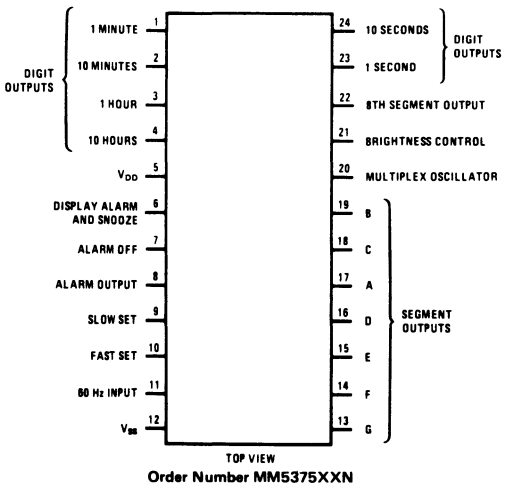
- 50/60 Hz operation
- Single power supply
- Low power dissipation
- 12/24 hour display format
- AM/PM indication
- Calendar register option
- Elapsed time register option
- 24-hour alarm setting
- All counters resetable
- Fast and slow set controls
- Power failure indication
- Brightness control capability
- No illegal time display at turn-on
- Alarm tone output
- Simple interface to gas-discharge displays and LED's
- 6 to 8 minute snooze alarm
- Internal digit multiplex oscillator
- Leading zero blanking
- Activity indicator
- 4 or 6 digit operation

applications

- Alarm clocks
- Desk clocks
- Automobile clocks
- Industrial clocks
- Military clocks

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5375XXN
See Package 18

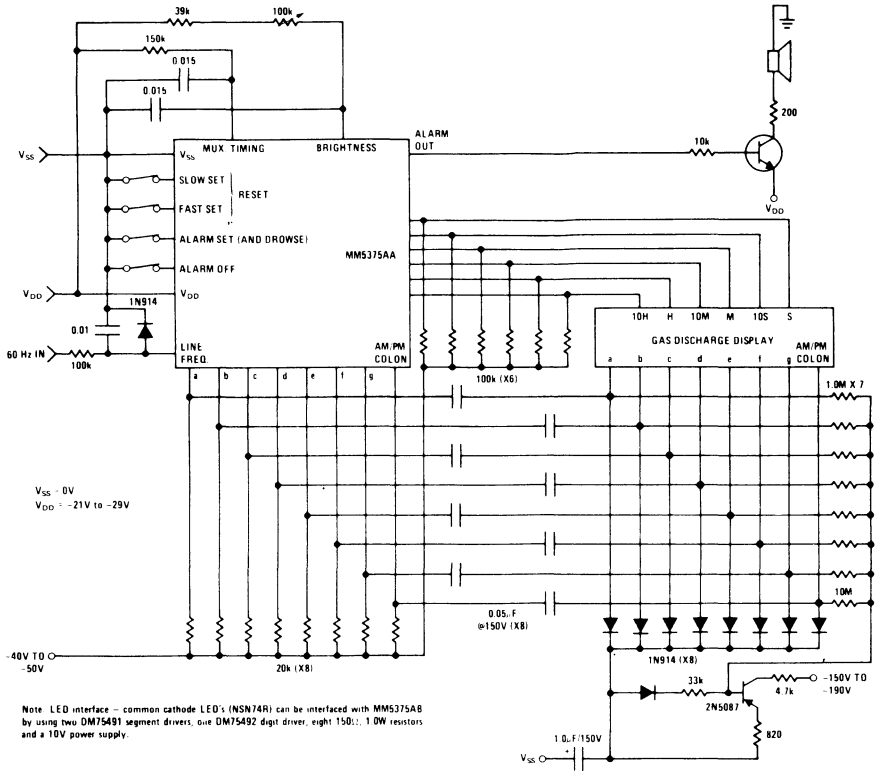


FIGURE 2. Typical Application

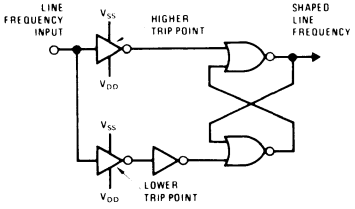


FIGURE 3. 60 Hz Shaping Circuit

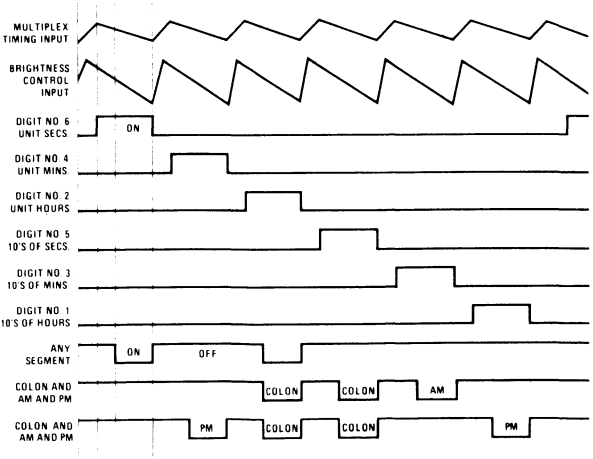


FIGURE 4. Output Timing Diagram

MM5736 MOS/LSI 6 digit calculator

general description

The MM5736 employs three working registers to provide add, subtract, multiply and divide functions. It includes on-chip key debounce and interfaces directly with the keyboard matrix as shown in Figure 2 and 3. A one-of-six output provides the strobe signals necessary to enable the appropriate digit for display; segment data for each digit appears during the appropriate strobe. See Figure 1 for digit and segment timing. Leading zero blanking has been incorporated to conserve battery life. Average battery life is estimated to be between 10 and 20 hours depending upon battery quality, operating schedule and the average number of digits displayed.

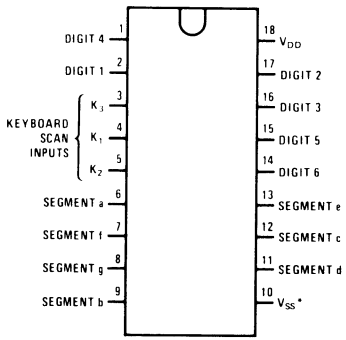
With the addition of a single-pole slide switch, a decimal point may be lit at an appropriate digit in the display; e.g., the third digit will present a dollars and cents format for users who generally use the calculator to balance checkbooks or keep track of supermarket expenditures. (Figures 2 and 3 indicate this feature using the NSN66A LED display, which has a decimal point between the second and third digits.)

features

- Six digit display
- Four functions (+, −, X, ÷)
- Chain operations
- Auto summing, convenient counting by any radix, and auto squaring
- Floating negative sign indicator for true credit balance
- Three different error indications
- Leading zero blanking
- On-chip oscillator uses no external components
- Effective keyboard bounce protection
- Interfaces with keyboard directly
- 9.0V battery operation with a typical power dissipation less than 30 mW—resulting in a battery life in excess of 15 operating hours with normal use

connection diagram

Dual-In-Line Package



TOP VIEW

*V_{SS} always most positive supply

Order Number MM5736N
See Package 16

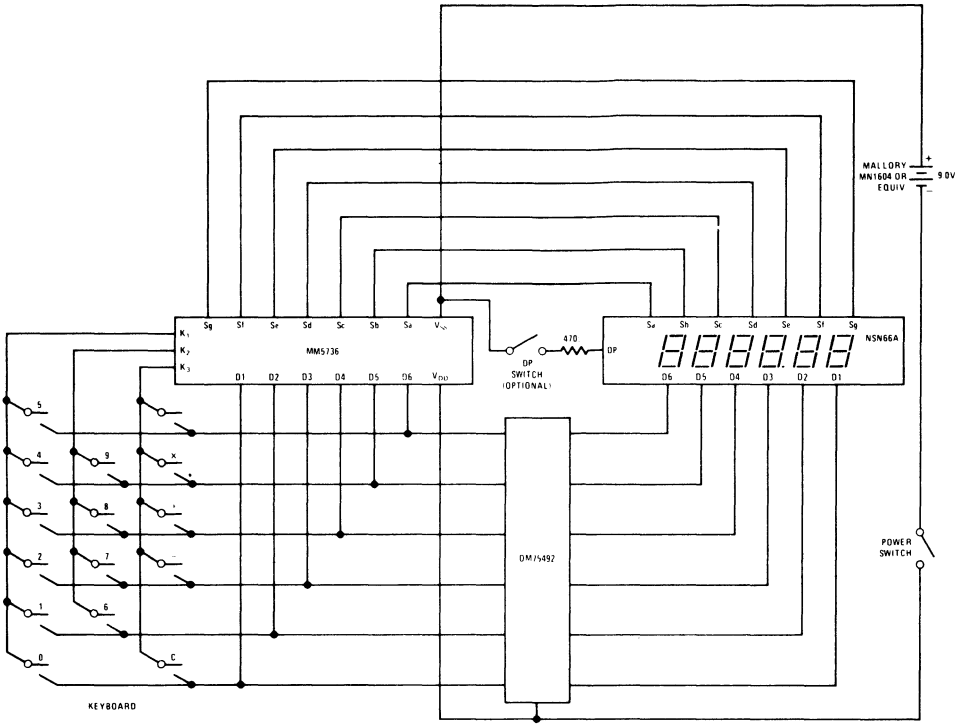


FIGURE 3. Optional Calculator Configuration with MM5736

keyboard bounce and noise rejection characteristics

The MM5736 calculator is designed to interface with low cost keyboards. These keyboards are usually the least desirable from a noise and false entry standpoint. When a key closure is sensed by the calculator, an internal timeout is started. Any peturbations which occur during the timeout will reset the timer to zero so that a key is only accepted as vaild after a noise-free time out period. Noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

Low cost conductor loaded elastomeric keyboards often have key-pressure versus contact resistance characteristics that can create almost continuous noise during "teasing" or low pressure key depressions. The MM5736 keyboard scanning circuitry can accept a series switch resistance up to 50 kΩ as a valid closure, which combined with the internal resettable debounce timer, insures reliable key operations under a variety of conditions and keyboards.

range of the calculator

The MM5736 is capable of displaying six significant positive digits and five negative digits:

$$-99999 \leq \text{Display} \leq +999999$$

The display scans from right (LSD) to left (MSD). Digit 1 time (Figure 1) corresponds to LSD.

error conditions

The following is a list of error conditions which are displayed by the MM5736. If any of these conditions occur, the machine automatically locks out all key entries except CLEAR.

Error	Display
(1) Too many numbers entered	EXXXXX
(2) Negative solution too large	EEXXXX
(3) Positive Solution too large	EXXXXX
(4) Divide by 0	EEEEEE

MM5738 calculator

general description

The MM5738 calculator was designed with "low system cost" as a major criterion. Through advanced design techniques National Semiconductor has been able to incorporate many desirable features into the MM5738 and still offer significant overall cost effectiveness, probably best emphasized by evaluating the additional components required to fabricate a competitors complete hand-held calculator.

Other than a single DM8864 digit driver, there are *NO* external components necessary to interface the MM5738 to the LED display, keyboard and 9.0V battery of a finished calculator. Figure 1 shows the keyboard matrix and interconnections of these elements.

The MM5738 uses the familiar algebraic notation performing addition, subtraction, multiplication division and percentage operations on positive or negative eight digit, floating point numbers. It is capable of doing chain or constant problems while retaining another number in an independent memory register. The contents of the memory register are only altered upon the depression of the *Memory Store* key and are unaffected by any clear or recall memory operations.

The MM5738 provides an on-chip key debounce circuit that interfaces directly with the appropriate keyboard matrix (Figure 1). While a digit driver is required, the MM5738 can drive the segments of most common cathode LED displays directly. The one-of-nine digit outputs provide the strobe signals necessary to enable the proper digit for display; segment data for each digit appears during the appropriate strobe (Figure 2). The ninth digit is used as a sign or error indicator, and in conjunction with the DM8864 digit driver, as a low voltage indicator. (The decimal point of the ninth digit is usually used as the low voltage indication alerting the user to the need for battery replacement in the near future, without interfering with his normal use of the calculator.) The negative sign always resides one position to the left of the most significant digit of negative numbers and therefore only appears in the ninth position when an eight digit negative number is being displayed.

Leading zero blanking and a display turnoff circuit have been incorporated into the MM5738 to conserve battery life. Battery life is estimated to be between 10 and 15 hours, depending upon battery quality, operating schedule and the average number of digits displayed.

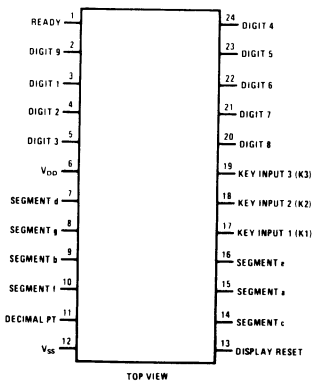
The *READY* pin from the MM5738 is an output signal used to indicate when the calculator is performing an operation. This signal may be helpful if the device is used in a system other than a calculator or for optimizing testing. It is possible to defeat the key debounce circuit for faster key entries.

features

- Full 8-digit capacity
- 5-functions (+, −, x, ÷, %)
- Chain operations
- 2-key memory
- Constant operations independent of memory
- Auto squaring
- Percent discount and tax operations
- Floating decimal point for ease of operation
- Floating negative sign indicator. Tracks most significant digit.
- Convenient algebraic key entry notation
- Leading zero blanking
- On-chip oscillator uses no external components
- Display turnoff (after 16 seconds) with no external components
- Requires only a digit driver to interface with an LED display
- Key debounce uses no external components
- Direct 9.0V battery compatibility

connection diagram

Dual-In-Line Package



Order Number MM5738N
See Package 18

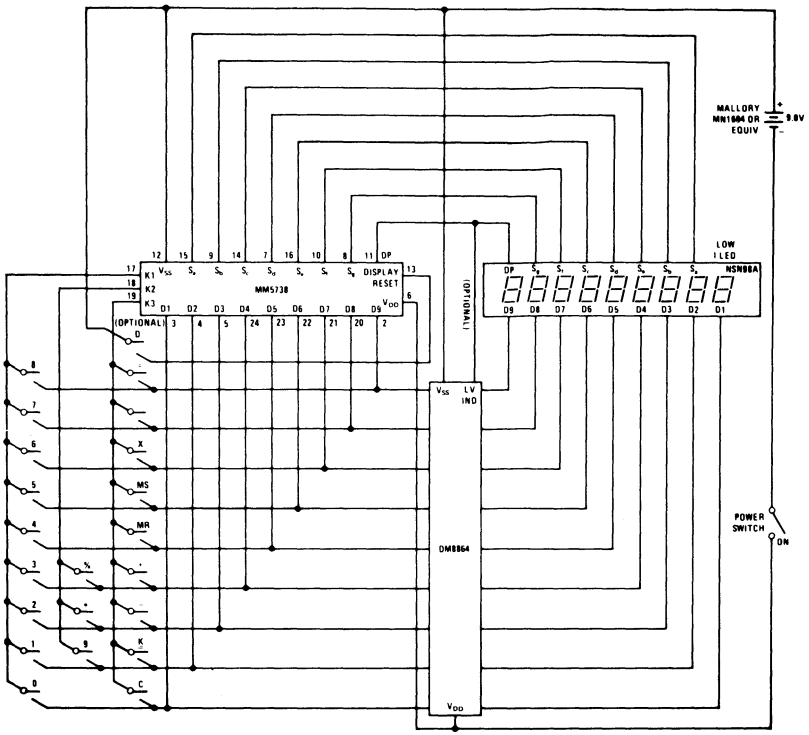


FIGURE 1. MM5738 Calculator with Low Voltage Indicator and Display

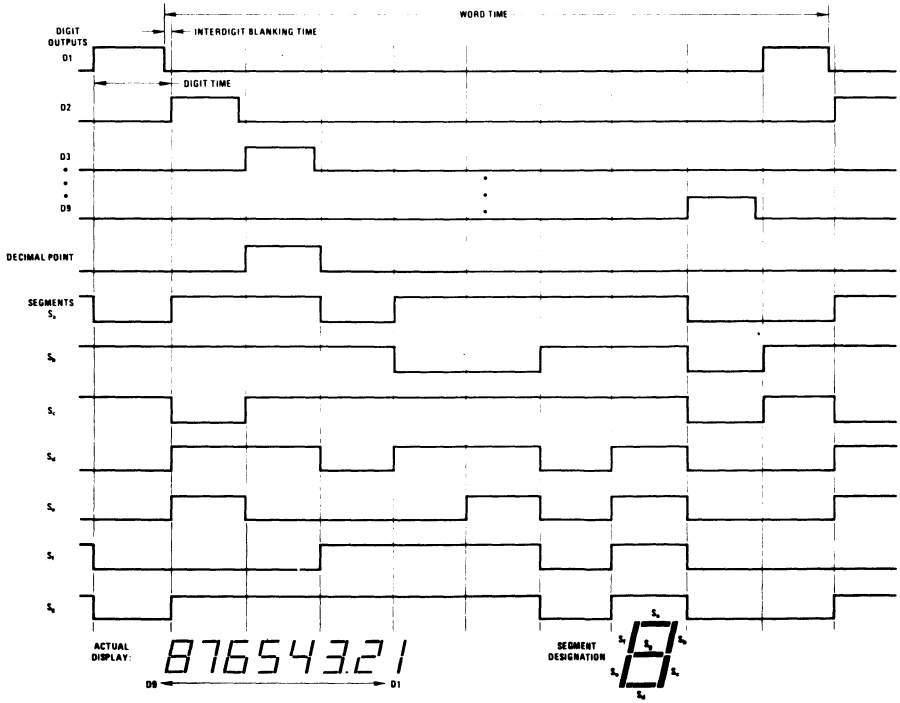


FIGURE 2. Display Timing Diagram

MM5739 calculator

general description

The MM5739 employs three working registers to provide add, subtract, multiply and divide functions. It includes on-chip key debounce and interfaces directly with the keyboard matrix as shown in Figure 2. While a digit driver is required, the MM5739 can drive the segments of most LED displays directly. A one-of-nine output provides the strobe signals necessary to enable the appropriate digit for display; segment data for each digit appears during the appropriate strobe. See Figure 1 for digit and segment timing. Leading zero blanking and a 16 second display turnoff circuit have been incorporated to conserve battery life. Battery life is estimated to be between 10 and 20 hours, depending upon battery quality, operating schedule and the average number of digits displayed.

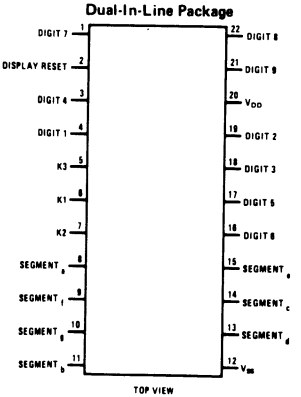
For the additional cost of a single pole slide switch, a decimal point may be lit at any convenient point in the display; i.e., zero decimal point or two decimal point position. (Figure 2 indicates the wiring for a decimal point in the dollars/cents position.) This would be helpful for users who are generally operating in an "adding machine" mode; e.g. housewives when balancing their checkbooks or keeping track of supermarket expenditures.

features

- 9-digit display
- 4-functions (+, −, x, ÷)
- Chain operations
- Auto summing, convenient counting by any radix, and auto squaring
- Floating negative sign indicator for true credit balance
- 3-different error indications
- Leading zero blanking
- On-chip oscillator uses no external components
- Display turnoff after 16 seconds with no external components
- Effective keyboard bounce protection
- Requires only a digit driver to interface with a LED display
- Interfaces with keyboard directly
- 9.0V battery operation with a typical power dissipation less than 35 mW—resulting in a battery life in excess of 15 hours with normal use.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5739N
See Package 17

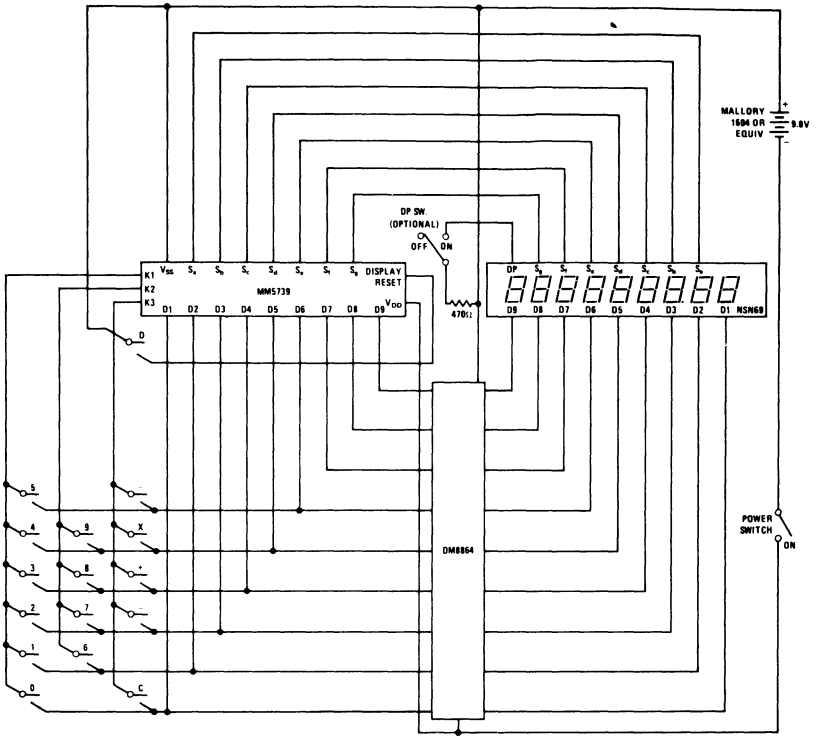


FIGURE 2a. Recommended MM5739 Calculator Schematic with Display Cutoff Feature

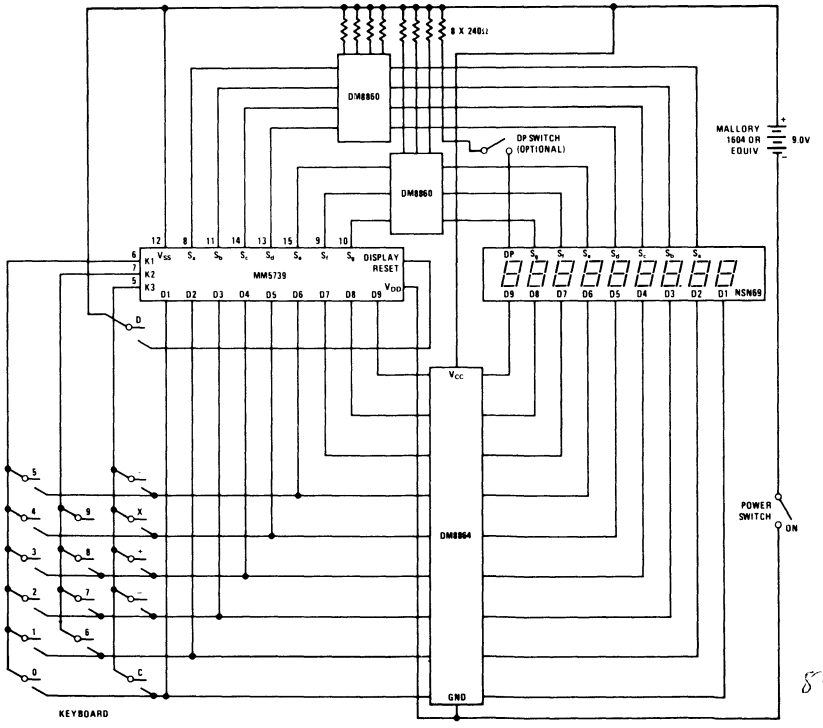


FIGURE 2b. Optional Calculator Schematic (with optional fixed decimal point and display cutoff feature)

MM2102
1024-bit fully decoded static random access memories

general description

The MM2102 family of 1024 word by one bit static random access read write memories are manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

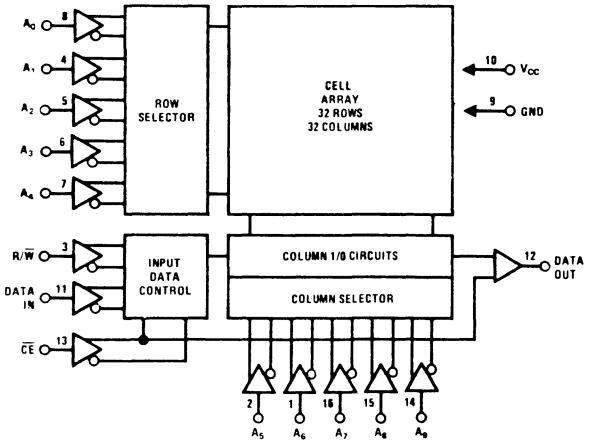
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 family ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

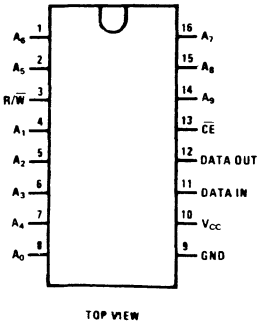
features

- Single +5V supply
- All inputs and output directly DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power 150 mW typ
- Fast access
  - MM2102 1μs
  - MM2102-1 500 ns
  - MM2102-2 650 ns
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- Low cost 16-pin Epoxy B package

block and connection diagrams



Dual-In-Line Package

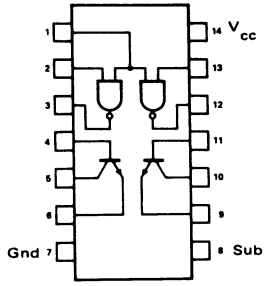


TOP VIEW

Order Number MM2102D, MM2102-1D or MM2102-2D
See Package 3

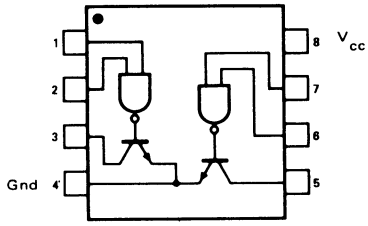
75450

The 75450 is a dual peripheral driver designed for use in systems that employ TTL or DTL logic. This circuit features two standard 7400 series gates and two uncommitted, high current, high voltage, npn output driver transistors.



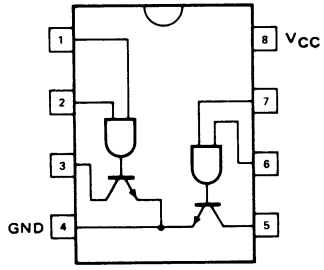
75451

The SN75451 dual peripheral driver is a versatile device designed for use in systems that employ TTL or DTL logic. This circuit contains dual AND drivers (positive logic) with the gate outputs internally connected to the npn output trnasistors.



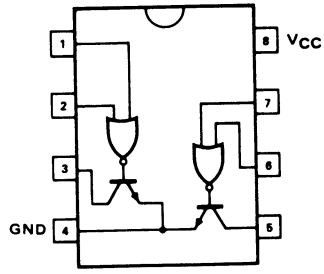
75452

The SN75452 dual peripheral driver is a versatile device designed for use in systems that employ TTL and DTL logic. These circuits are dual NAND drivers (positive logic) with the gate outputs internally connected to the NPN output transistors.



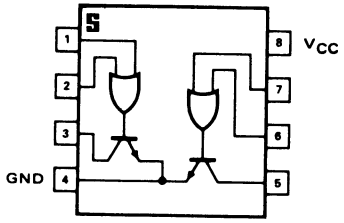
75453

The SN75453 dual peripheral driver is a versatile device designed for use in systems that employ TTL or DTL logic. These circuits are dual OR drivers (positive logic) with the gate outputs internally connected to the NPN output transistors.



75454

The SN75454 dual peripheral driver is a versatile device designed for use in systems that employ TTL or DTL logic. The circuits are dual NOR drivers (positive logic) with the gate outputs internally connected to the npn output transistors.



DM75491 MOS-to-LED quad segment driver
DM75492 MOS-to-LED hex digit driver

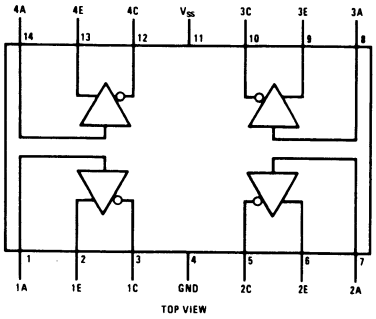
general description

The DM75491 and DM75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

features

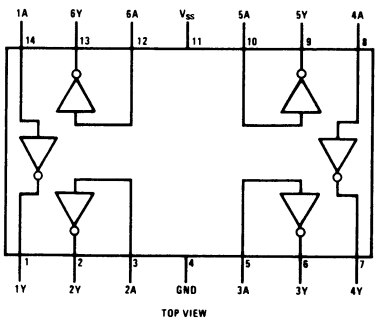
- Source or sink capability per driver (DM75491) 50 mA
- Sink capability per driver (DM75492) 250 mA
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

DM75491 Dual-In-Line Package



TOP VIEW

DM75492 Dual-In-Line Package



TOP VIEW

Integrated Electronics, Inc., P.O. Box 2022, Orange, CA 92669
Telephone: (714) 997-1673